

## RESEARCH IN PULSE WIDTH MODULATED HVDC TRANSMISSION

B T Ooi\*, F D Galiana\*, D McGillis\*\*\*\*, H C Lee\*, X Wang\*, Y Guo\*,  
J W Dixon\*\*, H L Makra\*\*\*, J Bélanger\*\*\*\*

\* McGill University, Canada  
\*\* Universidad Católica de Chile, Chile  
\*\*\* Institut de recherche d'Hydro-Quebec, Canada  
\*\*\*\* Hydro-Quebec, Canada

**ABSTRACT**

The advances of high power, high frequency, solid-state switches with gate "turn-off" capability (GTO's) are reaching a level when it is justified to initiate research and development in the PWM generation of HVDC. The paper presents results based on 1kVA experimental PWM converter and digital simulations, which show that: (1) the PWM HVDC system is technically realizable, (2) the MVA ratings can be raised for bulk power transmission, and (3) the performance improvement is sufficiently significant as to justify further investments in Research and Development.

**INTRODUCTION**

The advances of the pulse width modulation (PWM) technique in the motor-drive industries and the recent availability of high power, high frequency GTO's [1] suggest that the time is ripe to initiate research in the applications of PWM in HVDC. The technical challenge is to perfect the PWM station which can handle hundreds of KV and thousands of MVA. This paper takes the view that this expensive undertaking should be deferred until system studies show that there are benefits to be gained in such a change-over.

This paper is the culmination of several years of studies on the Voltage Source Type Converter [2-10] and the methods of increasing their MVA ratings [8,10]. This work is a continuation of the pioneering research of many predecessors [11-13]. The advances of solid-state technology will assure further investigations along the lines of force commutated HVDC.

**PART I VOLTAGE SOURCE TYPE BRIDGE CONVERTER**

Fig.1 shows the topology of the Voltage Source Type Bridge Converter, which is distinguished by the following features: (1) the capacitor  $C_n$  is across the dc link, (2) the inductors are on the ac side, (3) the valves with gate 'turn-off' capability (boxed 'V') have the current flow directed from the positive dc rail D to the negative rail E, (4) each valve has an antiparallel diode across it. It is assumed that the dc link voltage  $V_{cn}$  is always present and sufficiently high with respect to the ac line voltage so that the antiparallel diodes are normally reversed biased. The valves are triggered ON and OFF by logic signals to their gates from the PWM Control Block. The reader is referred to Ref.[2] for a detailed description of the operation of the Voltage Source Type Converter.

**Characteristics of Voltage Source Type Converter**

Fig.2 is an oscillogram showing: (a) the fundamental harmonic voltage, (b) an ac line current (c) the dc link current  $i_{ln}$ , and (d) the dc link current  $i_{2n}$  after filtering by the capacitor  $C_n$ , from a Voltage Source Type

Converter under PWM control. From inspection, one sees that the ac current is near sinusoidal and residual harmonics are in the high frequency end of the spectrum.

Fig.3 shows the results of an experiment in which the dc link voltage, and the amplitudes of the ac voltages and currents are kept constant but the power factor angle is varied. Fig.3 (a), (b) and (c) plot the dc link current, the real and the reactive power respectively as a function of power angle.

From Fig.3 (a) and (b) one sees that the Voltage Source Type Converter can operate with a constant unidirectional dc link voltage and power reversal is brought about by the reversal of the direction of the dc link current. In contrast, the conventional HVDC station operates with unidirectional dc link current and power reversal is achieved by reversal of the voltage polarity. The practical implication is that multi-terminal Voltage Source Type Converters can be connected in parallel at the dc terminals and power reversal can be easily implemented without the need of mechanical reversing switches.

From Fig.3 (c), it is apparent that the Voltage Source Type Converter can absorb both leading and lagging reactive power. In contrast, the conventional HVDC converter cannot operate with leading power factor.

**Part II PWM CONTROLS OVER VOLTAGE SOURCE TYPE CONVERTER**

Fig.4 shows the schematic by which the 3 analogue input voltage signals  $V_{modnc}$ ,  $\theta_{nc}$  and  $\omega_{nc}$  respectively control the voltage amplitude, the voltage angle and the frequency of the fundamental Fourier Series Component of the line-to-neutral voltage at each of the terminals A, B and C of the Voltage Source Type Converter. The design is based on a mixture of analogue (input and output signals are analogue) and digital circuitry.

Of the many varieties of PWM methods, the sinusoidal PWM (SPWM) [14] is chosen because it is simple to implement.

In Fig.4 the Block labelled SPWM Control accepts an analogue sinusoidal modulating waveform signal from each of the 3-phases and an analogue triangular carrier signal, and based on detecting the intersection points it generates gating signals to the valves of the bridge. The SPWM Control Block is well known and needs no further elaboration.

In the schematic of Fig.4, one sees that the 3 modulating waveforms and the carrier waveform are generated from the memories of the 4 EPROM's. The memory contents are converted from binary digital values by the digital to analogue (D/A) converters. In the example which was implemented, the fundamental period  $0 < \theta < 2\pi$ , was digitized into  $2^9=512$  parts and

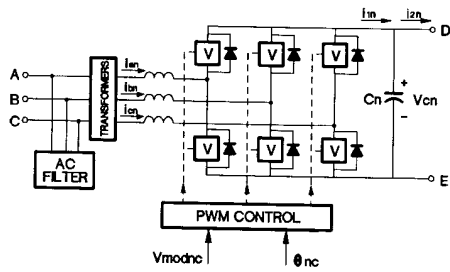


Fig.1: Schematic of Voltage Source Type Converter Bridge.

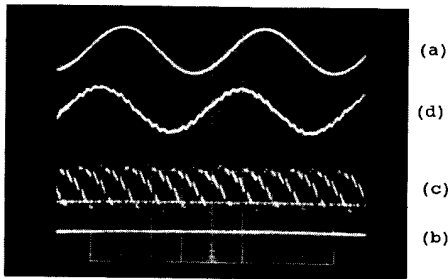


Fig.2: Steady-state waveforms of Voltage Source Type Converter under SPWM control: (a) Fundamental harmonic voltage at ac terminal, (b) ac line current, (c) dc link current  $i_{1n}$ , (d) dc link current  $i_{2n}$  after filtering by the dc link capacitor.

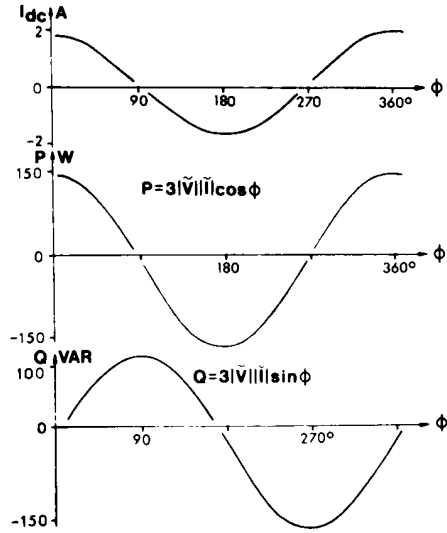


Fig.3: Steady-state characteristics as a function of phase angle, with ac voltage, ac current and dc link voltage kept constant. (a) dc link current, (b) real power (c) reactive power.

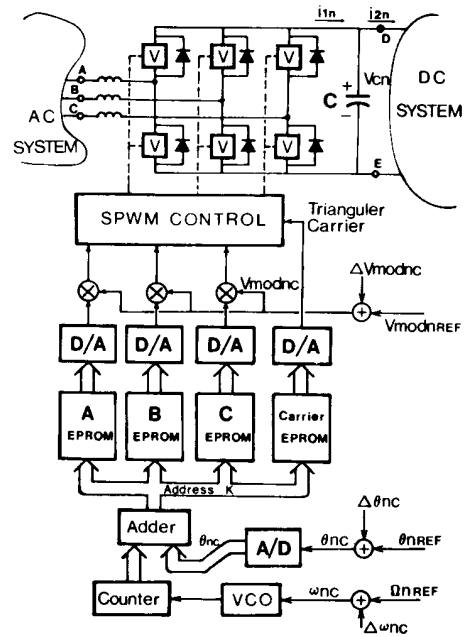


Fig.4: Schematic showing implementation of independent controls over voltage magnitude, voltage angle and frequency of Voltage Source Type PWM Converter.

corresponding to the addresses  $K=0,1,2...511$ , the A, B and C Eprom's contain binary values which are respectively proportional to  $\sin(2\pi[K/512])$ ,  $\sin(2\pi[(K/512)-(1/3)])$  and  $\sin(2\pi[(K/512)-(2/3)])$ . The carrier EPROM contains the digital information of 18 identical isosceles triangles.

As the number  $K$  is continually incremented by 1 with modulo 512, the digitized approximations of the balanced 3-phase sinusoidal waveforms and triangular carrier waveform are generated at the output of the digital to analogue converters (D/A's).

**Voltage Amplitude Control**

The Voltage Amplitude Control is achieved by multiplying the outputs of the D/A's of the A, B and C Eprom's by the analogue signal  $V_{modnc}$  as shown in Fig.4. Thus  $V_{modnc}$  determines the amplitude of the sinusoidal modulating waveform in Fig.5 and therefore modifies the positions of its intersections with the constant amplitude triangular carrier waveform.

**Voltage Angle Control**

As shown in Fig.4, the address  $K$  is obtained from the binary addition of two numbers. The first binary number comes from a binary counter of 9 bits (modulo 512). The second binary number comes from an analogue to digital converter (A/D) whose input is the analogue voltage signal  $\theta_{nc}$ . The signal  $\theta_{nc}$  therefore introduces an address displacement (which may be positive or negative) with respect to the address contained in the binary counter. Since  $K=0, 1, 2...511$ ,  $\theta_{nc}$  spans 0 to  $2\pi$ , the address displacement is basically a voltage angle displacement.

**Frequency Control**

The binary counter, just mentioned, counts the pulsed output of the Voltage Controlled Oscillator (VCO) whose analogue signal input  $\omega_{nc}$  determines the pulse rate. Thus  $\omega_{nc}$  controls the frequency at which the 4 EPROM's are cycled by the 9 bit binary counter.

**Reference Settings**

As shown in Fig.4, each of the 3 control inputs is the sum of a reference setting and another input for the introduction of feedback control. Thus

$$\begin{aligned} V_{modnc} &= V_{modncREF} + \Delta V_{modnc} \\ \theta_{nc} &= \theta_{ncREF} + \Delta \theta_{nc} \\ \omega_{nc} &= \omega_{ncREF} + \Delta \omega_{nc} \end{aligned}$$

**Voltage Angle Control of Real Power**

Fig.5 shows the results of an experiment in which the ac terminals of the Voltage Source Type Converter were connected to an ac bus through balanced inductive reactances which represented the transmission lines. The converter was rated at 1kVA and the controls were as given in Fig.4. Fig.5 demonstrates that the power of the Voltage Source Converter under voltage angle control is close to the approximate formula  $V_s V_r \sin(\delta) / X_l$ , where the sending end voltage,  $V_s$ , and the receiving end voltage,  $V_r$ , are kept constant and the receiving end power is controlled the voltage angle  $\delta$ .

**Part III MULTI-TERMINAL HVDC TRANSMISSION NETWORK**

In this section, it is shown that by using the voltage angle control, the exchanges of real power in the multi-terminal network can be handled easily by local feedbacks. This is achieved by two building blocks in the multi-terminal network:

- (1) the DC Voltage Regulator (VR) in Fig.6.
- (2) the Power Dispatcher (DISP) in Fig.7.

In each of the two building blocks, a negative feedback error signal is injected to the voltage angle terminal  $\Delta \theta_{nc}$  and the frequency terminal  $\Delta \omega_{nc}$  of Fig.4.

**DC Voltage Regulator**

In the block diagram of the Fig.6 and 7, the square with the label M represents the measurement transducers. In the DC Voltage Regulator of Fig.6, the DC link Voltage  $V_{cn}$  is measured and compared with the reference voltage  $V_{cnREF}$  and the negative feedback error  $\epsilon_{Vn}$  is applied to  $\Delta \theta_{nc}$  and  $\Delta \omega_{nc}$  in Fig.4. The voltage angle  $\theta_{nc}$  adjusts the power through the converter to ensure that the reference voltage is maintained.

**Power Dispatcher**

In the Power Dispatcher of Fig.7, the transducer in M measures  $P_n$ , the power through the converter, and compares it with the power reference  $P_{nREF}$ . The negative feedback error  $\epsilon_{Pn}$  is applied to  $\Delta \theta_{nc}$  and  $\Delta \omega_{nc}$  in Fig.4.

The feedback loop regulates the power through the Power Dispatcher. The power reference  $P_{nREF}$  can be positive (rectifier) or negative (inverter).

**Multi-terminal Power Exchange through Local Control**

Two 1kVA size converter units, fitted as a Voltage Regulator (VR) and a Power Dispatcher (DISP), were connected back-to-back to join two ac transmission systems as shown in Fig.8. The Power Dispatcher was made to operate as a rectifier by assigning to it a fixed positive

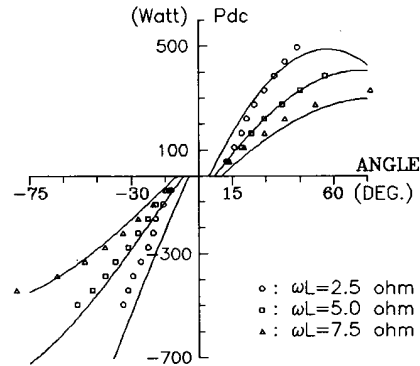


Fig.5: Power as a function of Voltage Angle for different values of line reactance. (positive power-rectifier, negative power-inverter).

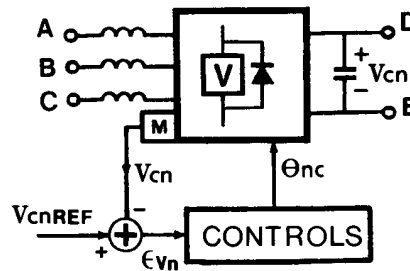


Fig.6: DC Voltage Regulator (VR).

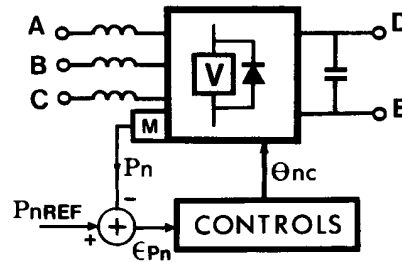


Fig.7: Power Dispatcher (DISP).

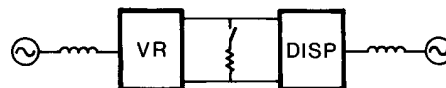


Fig.8: Schematic of multi-terminal connections for experimental results in Fig.9.

value of  $P_{PREF}$ . The DC Voltage Regulator (power slack) automatically assumed the role of an inverter. In the oscillogram in Fig.9, one sees this to be so in the initial portion, (a) the ac line current, and (b) the dc link output current (negative-inverter) of the DC Voltage Regulator; (c) the ac line current and (d) the dc link output current (positive-rectifier) of the Power Dispatcher.

The step power demand of a third converter station was simulated by closing a switch which connected a resistance across the dc link in Fig.8. This caused the transients which occurred in the middle of Fig.9. From Fig.9 (c) and (d) one sees that the Power Dispatcher maintains the power which has been assigned to  $P_{PREF}$ .

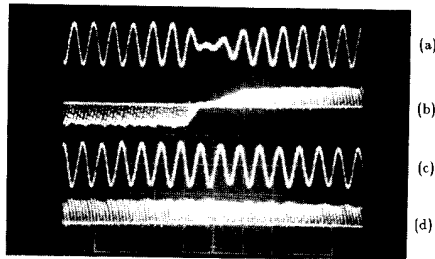


Fig.9: Transient response in multi-terminal connection: (a) ac current (VR), (b) dc link current (VR), (c) ac current (DISP), (d) dc link current (DISP).

From Fig.9 (a) and (b), one sees that the power demand of the "third station" was more than can be supplied by the Power Dispatcher and as a result the DC Voltage Regulator had to change from being an inverter to a rectifier. otherwise, the DC link voltage would collapse.

The experiment demonstrates that multi-terminal power exchanges, including power reversals can be handled very simply by local feedback controls.

**Part IV INCREASING MVA RATINGS FOR HVDC APPLICATIONS**

For HVDC applications it is necessary to connect GTO's (or similar devices) in series and in parallel to build up the voltage withstand limit and to increase the current carrying capabilities so that they function together as single valves in the modules of fig.1.

An additional approach, which our research [8,10] has found to be promising, is to increase the MVA ratings further by connecting the converter modules of Fig.1 in series and in parallel as shown in Fig.10. The block "F" represents the filters at the primaries of the transformers. The secondary of each of the 3-phase transformers is made up of  $N_f$  identical windings. Their terminals are organized into  $N_f$  sets of "floating" wye-connected, 3-phase ac buses. On each set of the 3-phase ac buses, one connects  $N_f$  identical modules of the converter of Fig.1 at the ac terminals a, b, c. The dc outputs d, e of each of the  $N_f$  modules are connected to a common dc bus and the dc link voltage developed across the dc link capacitor is  $V_{ei}$  ( $i=1,2,\dots,N_f$ ). Because

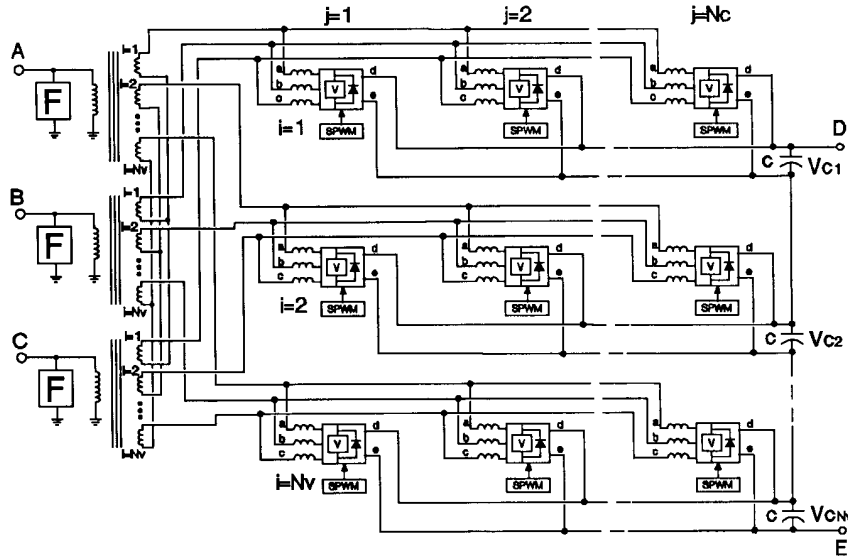


Fig.10: Multiple converter modules in series and in parallel to increase MVA ratings.

the secondaries of the transformers are "floating", the dc buses can be connected so that the dc link voltages add up in series. When the dc link capacitors are identical, the dc link voltage are evenly distributed.

The parallel connection of  $N_c$  modules increase the overall current rating. When the inductances are identical, the current is evenly distributed.

The valves in each converter are turned ON-OFF by the Sinusoidal PWM BLOCK as described in Part II.

**Harmonic Elimination**

Applying the findings of Ref [15,10], it is possible to add an improvement to the multiple connections of Fig.12. This consists of phase shifting the triangular carrier to each converter module by an amount which is an integral multiple of  $\theta_{sh}$ , as shown in Fig.11. It can be proved mathematically [10] and it has been demonstrated experimentally [10,15] that the Fourier series harmonics are eliminated up to a very high order.

As an example, Fig.12 shows the line currents from the detailed digital simulations of 7 converter modules connected in series.

There are two engineering implications from this method of harmonic elimination:

1. The PWM technique is implementable by low frequency switching devices such as GTO's and even force commutated thyristors.
2. With reduced switching rates, the switching losses come down.

The control circuitry which incorporate harmonic elimination by phase shifting the triangular carrier, is shown in Fig.13. It shows that the D/A outputs from the A, B, and C phase EPROM's are sent identically to all the  $N_c \times N_v$  SPWM BLOCK's.

The slight modification from Fig.13 is that each of the  $N_c \times N_v$  SPWM BLOCK's receives the triangular carrier signal from its own EPROM. The contents of these EPROM's are such that on being addressed successively by the binary counter, their D/A outputs trace out identical triangular waveforms which differ from each other by integral multiples of the phase shift  $\theta_{sh}$  as shown in Fig.11.

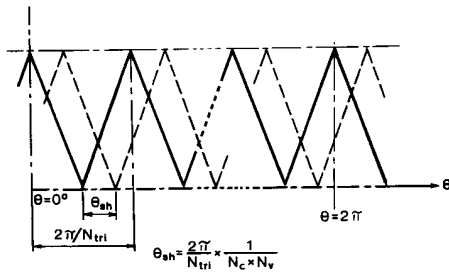


Fig.11: Method of phase shifting of triangular carrier for harmonic elimination.

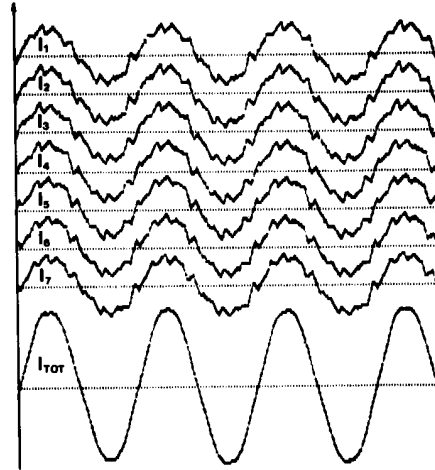


Fig.12: Current waveforms from digital simulation of 7 Converters whose triangular carriers are each phase shifted evenly in the period of the triangles. The total current shows significant elimination of harmonics.

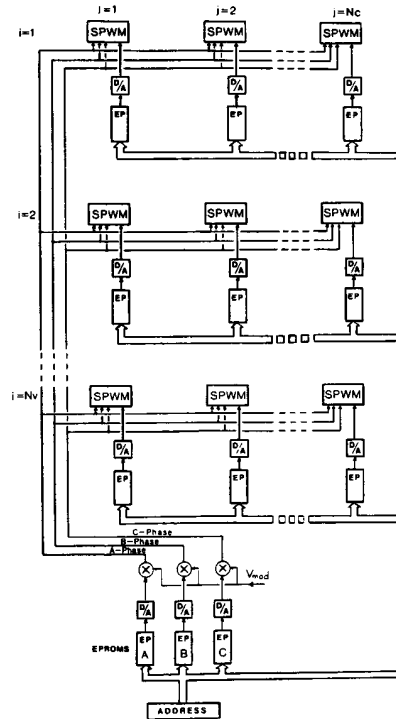


Fig.13: Schematic of the implementation of the SPWM strategy incorporating triangular carrier phase shifting for harmonic elimination.

**CONCLUSIONS**

From laboratory models of the Voltage Source Type Converters working as individual units and as multiple units in the multi-terminal HVDC configurations, it has been shown that a new generation of HVDC system based on PWM principles is technically feasible. From experiments of combining multiple modules in series and in parallel, the principle has been established by which the MVA ratings required of HVDC applications can be reached.

**ACKNOWLEDGMENTS**

The authors are grateful for financial support from the Natural Science and Engineering Research Council of Canada through a strategic Grant (Energy) and the Ministry of Education, Province of Quebec, through an FCAR grant.

**REFERENCES**

1. B.K. Bose, "Evaluation of modern power semiconductor devices and future trends of converters", IEEE-IAS Annual Meeting Conference Record, 1989, pp.790-797.
2. B.T. Ooi, J.C. Salmon, J.W. Dixon, A.B. Kulkarni, "A 3-Phase Controlled Current PWM Converter with Leading Power Factors". IEEE Trans., Vol.IA-23, Jan./Feb. 1987, pp.78-84.
3. B.T.Ooi, J.W.Dixon, A.B.Kulkarni, M.Nishimoto, "An Integrated AC Drive System Using a Controlled Current PWM Rectifier/ Inverter Link", IEEE Trans., Vol.PE-3, No.1, Jun. 1988, pp.64-71.
4. J.W. Dixon, A.B. Kulkarni, M. Nishimoto and B.T. Ooi, "Characteristics of a Controlled-Current PWM Rectifier-Inverter Link ", IEEE Trans., Vol.IA-23, No.6, Nov./Dec. 1987, pp.1022-1028.
5. M. Nishimoto, J.W. Dixon, A.B. Kulkarni and B.T. Ooi, "An Integrated Controlled-Current PWM Rectifier Chopper Link for Sliding Mode Position Control", IEEE Trans., Vol.IA-23, No.5, Sept./Oct. 1987, pp.894-900.
6. A.B.Kulkarni, M.Nishimoto, J.W.Dixon and B.T.Ooi, "Transient Tests on a Voltage Regulated Controlled Current PWM Converter", IEEE Trans., Vol.IE-34, No.3, Aug. 1987, pp.319-324.
7. J.W. Dixon and B.T. Ooi, "Indirect Current Control of a Unity Power Factor Sinusoidal, Current Voltage Source Type, 3-Phase Rectifier", IEEE Trans. Vol.IE-35, No.4, Nov. 1988, pp.508-514.
8. J.W. Dixon and B.T. Ooi, "Series and Parallel Operation of Hysteresis Current Controlled PWM Rectifiers", IEEE Trans. Vol.IA-25, No.4, July/Aug. 1988 pp.644-651.
9. B.T.Ooi, Pulse Width Modulation Power Transmission, U.S. Patent No. 4941079, filed Feb. 13, 1989.
10. J.W. Dixon and B.T. Ooi, "Dynamically Stabilized Indirect Current Controlled SPWM Boost Type Three Phase Rectifier", IEEE Industrial Application Society Annual Meeting, Oct. 1988.
11. J.Reeve, J.A.Barron and G.A.Hanley, "A Technical Assessment of Artificial Commutation of HVDC Converters with Series Capacitors", IEEE Trans., Vol.PAS-87, No.10, Oct. 1968, pp.1830-1846.
12. A.M.Gole and R.W.Menzies, "Analysis of Certain Aspects of Force Commutated HVDC Inverters", IEEE Trans., Vol.PAS-100, No.5, May 1981, pp.2258-2262.
13. H.M.Turani, R.W. Menzies and D.A. Woodford, "Feasibility of DC Transmission with Forced Commutation to Remote Loads", IEEE Trans., Vol.PAS-103, June 1984, pp.1256-1262.
14. B.M. Bird and K.G. King "An Introduction to Power Electronics" John Wiley and Sons 1983. pp. 198-202.
15. J. Holz, W. Lotzkat and K.H. Werner, "A high power multi transistor-inverter uninterruptible power supply system." IEEE Power Electronics Specialist Conference (Vancouver, Canada) June 1986, pp.311-326.