

Series and Parallel Operation of Hysteresis Current-Controlled PWM Rectifiers

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Abstract—Different strategies for series and parallel connections of the hysteresis current-controlled PWM rectifier have been investigated by experimental tests, digital computer simulations, and analyses. Each rectifier unit delivers near-sinusoidal current waveforms at unity (or even leading) power factor. Of particular concern are the questions of i) system stability, ii) the capability of the modular units to share voltage (series connection) and current (parallel connection) under steady-state and transient operation, and iii) sensitivity of performance characteristics to component tolerances. Experimental tests are based on 1-kW bipolar transistor modular units.

INTRODUCTION

BECAUSE naturally commutated converters form a significant fraction of the load on a utility system, their poor power factor and harmonic pollution have become sources for concern. These problems and the methods leading toward their improvement have recently been discussed by Divan and Barton [1].

This paper follows the solution based on the hysteresis current-controlled PWM converter which was originally conceived for inverter drive applications [2]–[5]. Operated as a rectifier, it has been shown to be capable of delivering near sinusoidal current waveform with unity and even leading power factor [6]. By incorporating an outer voltage feedback loop, the rectifier can be made into a stand-alone regulated voltage source with fast response to bidirectional power demands [8]–[9].

Unfortunately, for several years to come, the power ratings of the PWM rectifiers will be limited by the low voltage and the low current ceilings of commercially available fast-switching forced-commutated power electronic switches (bipolar transistors, GTO's, power FET's).

Looking at the historical development of thyristor technology [10], one sees series and parallel connections as the means of increasing ratings. The approach taken in this study consists of considering the PWM bridge converter described in [2]–[9] as a modular unit. The rating of each modular unit may be modest but is considered sufficient to justify the cost of its

current and voltage sensors and local controls. The study undertaken consists of considering the series and parallel connections of these modular units.

Two configurations labeled Type A and Type B, have been examined.

Type Description

- A independent local control
- B common switching control

Each modular unit (see Fig. 1) is autonomous in that it has its inner hysteresis current-control feedback loop, which requires at least two current sensors, and an outer voltage-regulator feedback loop, which requires one voltage sensor. The Type A (see Figs. 2 and 3) configuration consists simply of connecting these autonomous units together. The goal, of course, is to lower costs by reducing component count. Type B (see Figs. 8 and 13) does not need the local voltage feedback and the hysteresis current feedback in each unit.

In the previous work [6]–[9], the mathematical model of the basic modular unit of Fig. 1 has been thoroughly tested against experimental measurements under steady-state and transient conditions. For this reason, the composite behavior of Type A can be predicted with confidence from mathematical analysis. All the same, the predictions have been verified by digital simulations and, in critical cases, by experimental tests.

The conclusions of Type B are drawn entirely from digital simulation and experimental testing as its mathematical model must still be completely justified experimentally. Type B is an exciting finding as it offers significant savings in the components.

RECTIFIER MODULE

The rectifier module of Fig. 1 has been fully described in [6]–[9]. The current waveform templates are taken from voltage transformers, filtered and phase-shifted. The template waveforms are then multiplied by the amplitude control to form the reference currents. By hysteresis current control, the switchings of the bipolar transistors ensure that the currents measured by the transducers track the reference currents within the tolerance band.

Mathematical Model of the n th Module

In this paper it is assumed that the outer voltage regulator loop is a proportional controller. The control law of the rms ac phase current is

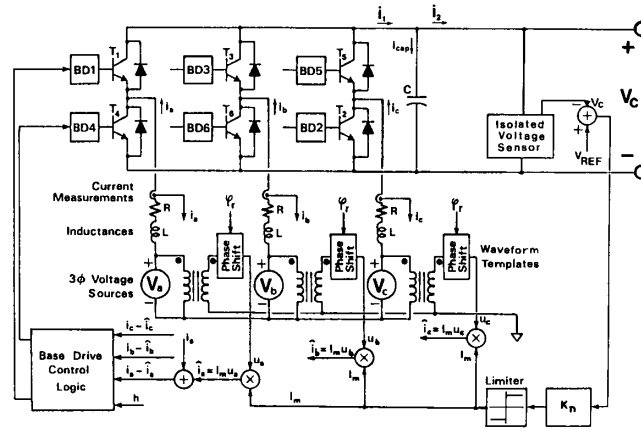
$$I_n = K_n (V_{REF} - v_{cn}) \quad (1)$$

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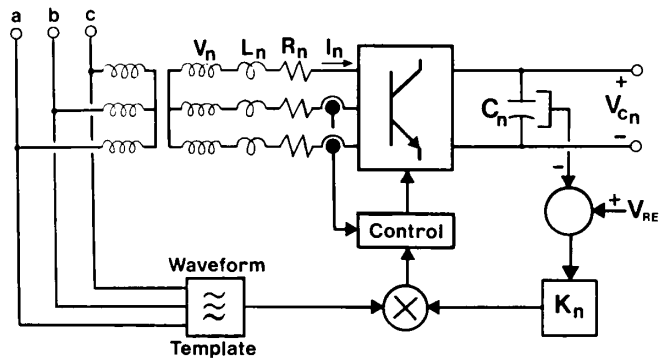
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(a)



(b)

Fig. 1. Basic hysteresis current-controlled PWM rectifier. (a) Detail circuit. (b) Diagrammatic representation.

where

- K_n transfer gain A/V,
- V_{REF} reference voltage,
- v_{cn} dc link voltage of n th module.

Based on the power balance equation and assuming unity power factor operation, the dc link output power is

$$i_{1n} \cdot v_{cn} = 3 \left[V_n I_n - R_n I_n^2 - \frac{d}{dt} \frac{1}{2} L_n I_n^2 \right] \quad (2)$$

where

- V_n rms phase voltage,
- i_{1n} local average dc link current output,
- R_n per-phase resistance,
- L_n per-phase inductance.

Kirchhoff's current law applied to the node of the dc link capacitance yields:

$$C_n \frac{dv_{cn}}{dt} = i_{1n} - i_{2n} \quad (3)$$

where i_{2n} is the dc link output local average current.

TYPE-A CONFIGURATION

Series Connected-Type A

As shown in Fig. 2, the series-connected Type A consists of connecting the autonomous modular units of Fig. 1 in series. The floating transformer secondaries allow the dc link voltages to be added to form the output V_{out} :

$$V_{out} = \sum_{n=1}^N v_{cn} \quad (4)$$

The output current i_{2n} is common through each unit:

$$i_{2n} = i_2 \quad n = 1, 2, \dots, N \quad (5)$$

and the output power is

$$P_{out} = i_2 \sum_{n=1}^N v_{cn} \quad (6)$$

The dynamic equation of each module is obtained by

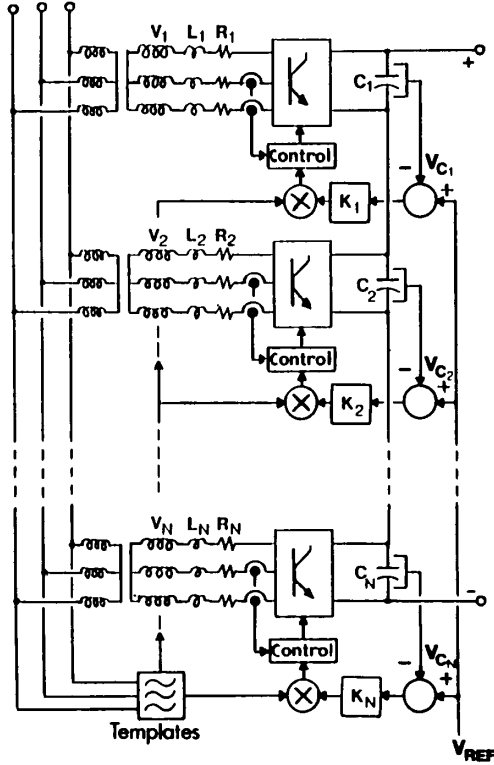


Fig. 2. Series-connected Type A.

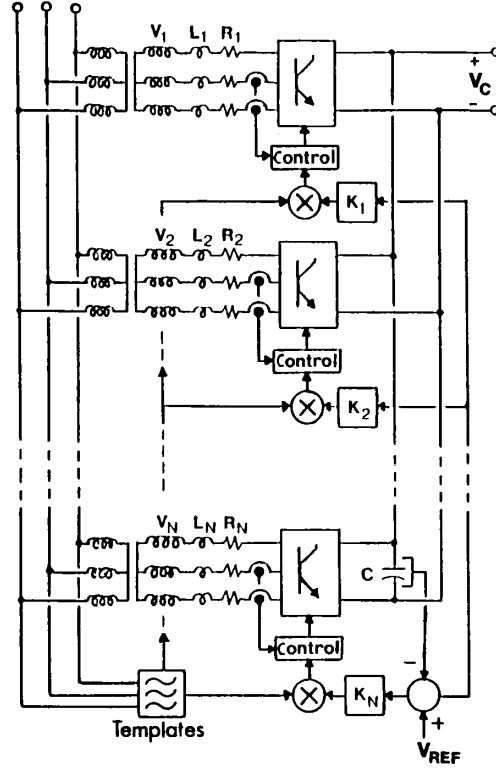


Fig. 3. Parallel-connected Type A.

combining (1), (2), and (3), and this yields:

$$\frac{dv_{cn}}{dt} = \frac{3V_n K_n (V_{REF} - v_{cn}) - 3R_n K_n^2 (V_{REF} - v_{cn})^2 - i_{2e} v_{cn}}{C_n v_{cn} - 3K_n^2 L_n (V_{REF} - v_{cn})} \quad (7)$$

$n = 1, 2 \dots N.$

Applying the standard technique of small perturbation linearization of (7) about the equilibrium and assuming that $\Delta i_2 = 0$, one obtains

$$\frac{d\Delta v_{cn}}{dt} = -\frac{1}{T_n} \Delta v_{cn} \quad (8)$$

$$T_n = \frac{C_n V_{cne} - 3K_n L_n I_{ne}}{3K_n [V_n - 2R_n I_{ne}] + i_{2e}} \quad (9)$$

and V_{cne} and i_{2e} are the equilibrium operating values of v_{cn} and i_2 , and

$$I_{ne} = K_n (V_{REF} - V_{cne}). \quad (10)$$

As has been noted in [9], the time constant T_n must be positive, and this requires that both the numerator and the denominator in [9] be positive. As discussed in [9], the positivity of the numerator sets the limit of stable operation to

$$I_{ne} < \frac{C_n V_{cne}}{3K_n L_n} \quad n = 1, 2 \dots N. \quad (11)$$

The positivity of the denominator requires that

$$I_{ne} < \left(V_n + \frac{i_{2e}}{3K_n} \right) / 2R_n. \quad (12)$$

Approximate Formulae

As the rigorous solution of the steady-state voltages V_{cne} and currents i_{2e} is complicated, one may use the approximations based on the facts that i) K_n is usually chosen to be large so as to yield little voltage droop, and ii) R_n is usually very small. One obtains the approximate formulae

$$V_{cne} \approx V_{REF} \quad (13)$$

$$I_{2e} \approx \frac{P_{out}}{NV_{REF}} \quad (14)$$

$$V_{out} \approx NV_{REF}. \quad (15)$$

Comments

The stability problem is one of considering if the operating point (V_{cne}, i_{2e}) , defined by the load and the remaining units, will yield a positive number as a time constant in (9). As this is a straightforward problem, one expects no surprises in this configuration. All the same, digital simulation studies have been performed on two units of 66-kW module for step power reversal from inverter operation ($i_2 = -100$ A dc) to rectifier operation ($i_2 = +100$ A dc). Fast stable response with good

sinusoidal current waveform at unity power factor were obtained for the capacitor size $C_1 = C_2 = 1000 \mu\text{F}$, which is near to the theoretical stability limit. The parameters of the 66-kW units used in the simulation studies are $V_n = 220 \text{ V ac}$, $R_n = 0.1 \Omega$, $L_n = 0.001 \text{ H}$, $K_n = 2 \text{ A/V}$, $V_{\text{REF}} = 660 \text{ V dc}$, hysteresis band = 10 A.

PARALLEL-CONNECTED TYPE A

The independent three-phase transformers for each modular unit in Fig. 3 have been drawn to be consistent with Fig. 2. In the parallel connection there is no compelling reason to "float" the secondaries. In this configuration, the dc-link output voltage is common, so that

$$v_{cn} = v_c \quad n = 1, 2 \cdots N. \quad (16)$$

The steady-state power balance requires that

$$P_{\text{out}} = 3 \sum_{n=1}^N [V_n I_n - R_n I_n^2]. \quad (17)$$

Substituting (1), one has

$$P_{\text{out}} = 3 \sum_{n=1}^N [V_n K_n (V_{\text{REF}} - V_{ce}) - R_n K_n^2 (V_{\text{REF}} - V_{ce})^2] \quad (18)$$

where V_{ce} is the equilibrium dc link voltage.

Based on (17) and (18), V_{ce} can be solved from the quadratic:

$$aV_{ce}^2 + bV_{ce} + c = 0 \quad (19)$$

where

$$a = 3 \sum_{n=1}^N R_n K_n^2 \quad (20)$$

$$b = 3 \sum_{n=1}^N [V_n K_n - 2R_n K_n^2 V_{\text{REF}}] \quad (21)$$

$$c = P_{\text{out}} + 3 \sum_{n=1}^N [R_n K_n^2 V_{\text{REF}}^2 - V_n K_n V_{\text{REF}}]. \quad (22)$$

The dynamic power balance equation is

$$v_c C \frac{dv_c}{dt} + P_{\text{out}} = 3 \sum_{n=1}^N \left[V_n I_n - R_n I_n^2 - \frac{d}{dt} \frac{1}{2} L_n I_n^2 \right]. \quad (23)$$

Substituting (1) into (23), and following the same small-signal linearization about the equilibrium voltage V_{ce} , one obtains the system linearized dynamic equation

$$\frac{d\Delta v_c}{dt} = -\frac{1}{T_e} \Delta v_c \quad (24)$$

where the time constant is

$$T_e = \frac{CV_{ce} - 3(V_{\text{REF}} - V_{ce}) \sum_{n=1}^N L_n K_n^2}{3 \left[\sum_{n=1}^N V_n K_n - 2(V_{\text{REF}} - V_{ce}) \sum_{n=1}^N R_n K_n^2 \right]}. \quad (25)$$

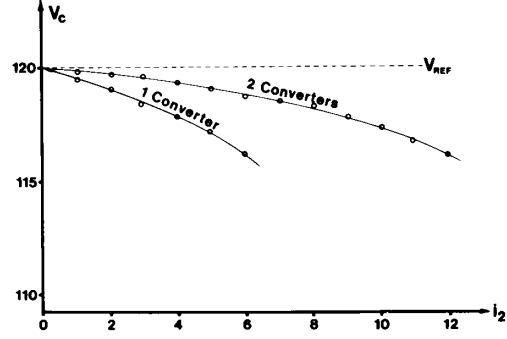


Fig. 4. Voltage regulation curve; parallel-connected Type A. DC link voltage as function of dc link current. Points—experiment. Lines—theoretical predictions.

For stable operation, T_e must be positive, and this requires both the expressions in the numerator and the denominator to be positive. For fast response, T_e is desirably a brief time constant.

Experimental Tests

The following experimental tests were performed on two identical laboratory rectifier units in order to provide spot-checks on the correctness of the analytical derivations.

Regulation Curve

Fig. 4 compares the dc link voltage regulation curve of a single rectifier in proportional feedback with that of two rectifiers. The abscissa consists of the total load current

$$i_2 = \sum_{n=1}^N i_{2n}.$$

The experimental points show excellent agreement with theoretical predictions based on the solution of (19).

From a practical viewpoint, one sees that parallel connection improves the voltage regulation of the proportional feedback controller.

Feedback Stability Limit

As discussed in [9], the time constant of (9) and (25) must be positive for the system to be stable. One sees that the time constant becomes negative when the numerators of (9) and (25) become negative. This form of instability is likely to be encountered before the instability associated with the denominator. For identical modular units ($L_n = L_r$, $n = 1, 2 \cdots N$) and identical feedback transfer gains ($K_n = K_p$, $n = 1, 2 \cdots N$), the stability limit based on the numerator of (25) being equal to zero is

$$I = \frac{CV_{ce}}{3NL_r K_p}. \quad (26)$$

Fig. 5 plots the rms phase current of each module in the ordinate. The theoretical limits of (26) are shown as straight lines. The experimental points (obtained by increasing the load until the oscillograms of the phase currents begin to distort and

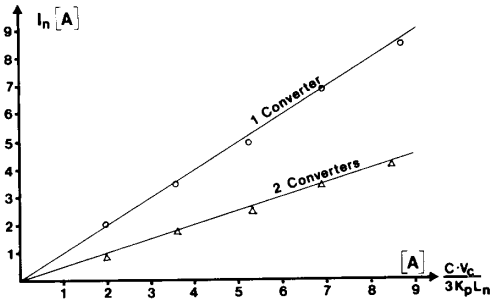


Fig. 5. Proportional control feedback stability limit. Parallel-connected Type A. Comparison of single and two parallel units. Points—experiment. Lines—theoretical predictions.

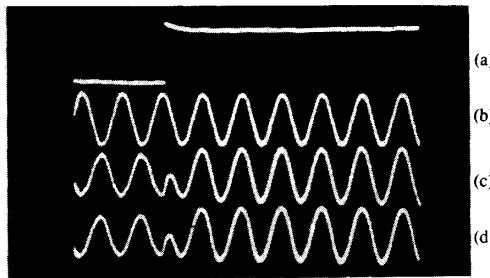


Fig. 6. Step reversal of power, from inverter to rectifier. Parallel-connected Type A. (a) DC link current, i_2 , -10 to +10 A dc. (b) AC phase voltage, $V_1 = 40$ V rms. (c) AC phase current, $n = 1$; from -4.5 to 6 A rms. (d) AC phase current, $n = 2$; from -4.5 to 6 A rms.

wobble from the sinusoidal waveforms) show excellent agreement with the predictions.

The formula in (26) and the results in Fig. 5 point to the fact that in order to increase the power rating by N , the dc link capacitance must also be increased by N .

Reversal-of-Power Test

Fig. 6 is a record of an experiment of power reversal (inverter to rectifier) from -10 to -10 A dc. The phase currents of the two modules are almost identical. Attention is drawn to i) unity power factor operation, ii) the good sinusoidal waveforms, and iii) the current sharing capability in steady state and in transient.

Unbalance Component Test

The reversal-of-power test was repeated for different values of inductive reactances in the two test modules: $X_1 = 2.5 \Omega$, $X_2 = 5 \Omega$. The details of the phase current in the two modules are shown in Fig. 7. The test confirms that the feedback loops enforce current sharing in spite of unbalances in the system components.

Laboratory Test Units

The laboratory rectifier modules were rated at $V_{ce} = 120$ V dc, $i_{2e} = 10$ A dc. In the tests of Figs. 4, 5, and 6, the parameters were $V_n = 40$ V ac, $R_n = 1 \Omega$, $X_n = 2.5 \Omega$, $K_n = 2$ A/V for $n = 1, 2 \dots N$, $C = 12$ mF.

The parameters remain the same for the test of Fig. 7 except for the deliberate unbalance in phase reactances.

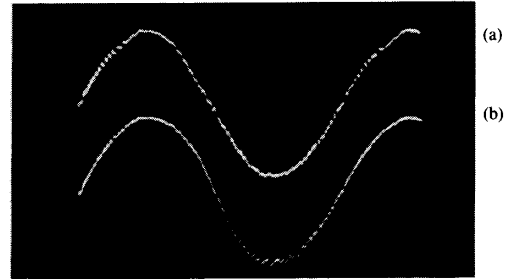


Fig. 7. Unbalance components test, parallel-connected Type A, $X_1 = 2.5 \Omega$, $X_2 = 5 \Omega$. (a) AC phase current, unit $n = 1$ -6 A rms. (b) AC phase current, unit $n = 2$ -6 A rms.

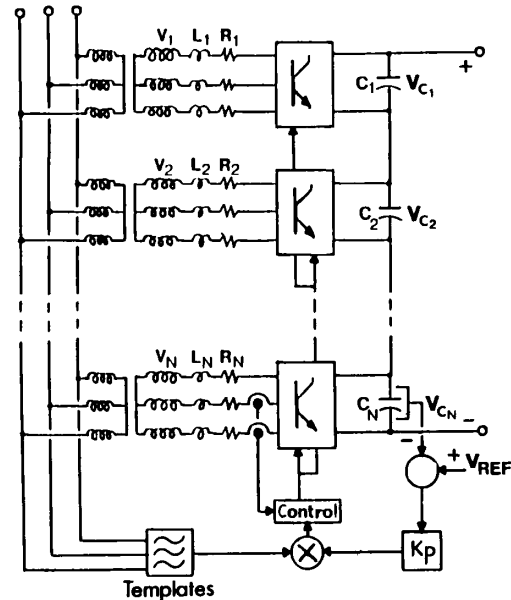


Fig. 8. Series-connected Type B.

TYPE-B CONFIGURATION

In the Type-B configuration of Figs. 8 and 13, the master unit ($n = N$) is identical to the original module of Fig. 1 and is stable provided T_N of (9) is positive. The slave units ($n = 1, 2 \dots N - 1$) are in open loop. The slave units receive logic commands from the master so that the power electronic switches in the bridge turn ON and OFF in unison with the corresponding switches of the master. Thus the voltage at one phase of each of the modules will have identical patterns such as shown in the oscillogram of Fig. 9.

In a Fourier analysis the fundamental component of the voltage can be represented by a phasor $V_{mod n}$ ($n = 1, 2 \dots N$).

The magnitude of the phasors are related to the master by the relationship

$$|\vec{V}_{mod n}| = \frac{v_{cn}}{v_{CN}} |\vec{V}_{mod N}| \quad (n = 1, 2 \dots N-1) \quad (27)$$

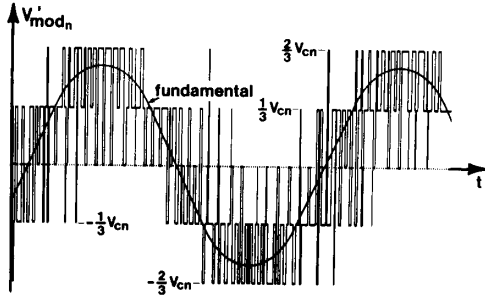


Fig. 9. Simulated waveform of phase voltage of one rectifier terminal and its fundamental Fourier component for Type B.

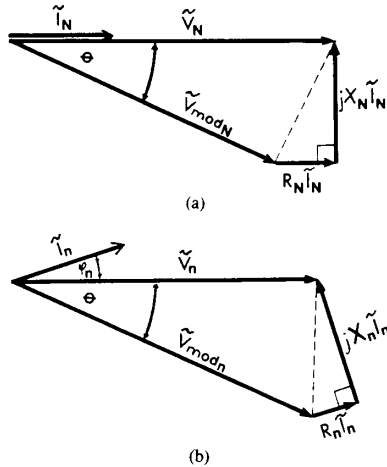


Fig. 10. Voltage and current phasor diagram relating fundamental harmonic component. (a) Master, unity power factor operation. (b) Slave n .

and they have the same phase angle as the master:

$$\theta_n = \theta_N \quad (n = 1, 2 \dots N-1). \quad (28)$$

In the master unit, it is the phase current magnitude I_N that is being controlled by the hysteresis current feedback. The voltage phasor diagram of the fundamental harmonic, as depicted in Fig. 10(a), shows how $\tilde{V}_{mod N}$ is related to \tilde{V}_N , \tilde{I}_N , and the impedance $\tilde{Z}_N = R_N + jX_N$.

The control of the slave units is through $\tilde{V}_{mod n}$, which is related to $\tilde{V}_{mod N}$ through (27) and (28).

One sees from the voltage phasor diagram of Fig. 10(b) that the current \tilde{I}_n is determined by $\tilde{I}_n \tilde{Z}_n$, which is the closing side of the triangle formed by \tilde{V}_n and $\tilde{V}_{mod n}$.

The analysis is too long to be included here. In this paper, only the experimental results on the 1-kW size modules are reported and they point to the encouraging news that i) Type B is stable both in the rectifier and the inverter regimes of operation, ii) series and parallel connections are possible, and iii) the ac phase currents are near sinusoidal at unity power factor.

SERIES-CONNECTED TYPE B

In the laboratory tests of the Type-B configuration of Fig. 8, only a single slave is controlled by the master.

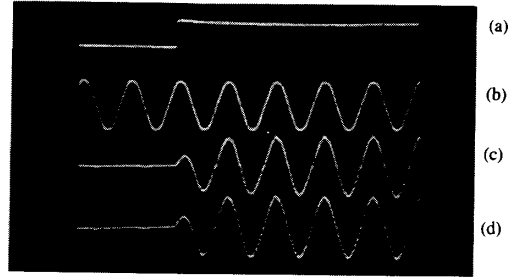


Fig. 11. Step response for series-connected Type B. (a) DC link current demand, 0 to +8 A dc rectifier. (b) AC phase voltage, $V_1 = 40$ V rms. (c) Phase current, slave, I_1 from 0 to 6 rms. (d) Phase current, master, I_2 from 0 to 6 A rms.

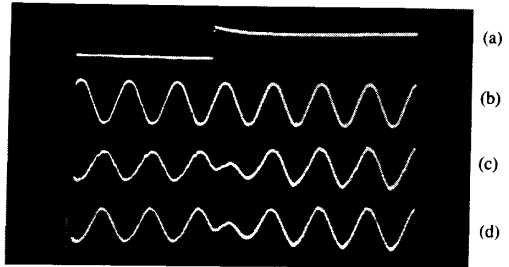


Fig. 12. Step power reversal of series connected Type B. (a) DC link current demand, from -5 to $+5$ A dc. (b) AC phase voltage, $V_1 = 40$ rms. (c) Phase current, slave, from -4.5 to 6 A rms. (d) Phase current, master, from -4.5 to 6 A rms.

Step Response Test

The photograph in Fig. 11 shows the response to a step demand of the dc-link output current i_2 , from 0 to 8 A dc.

In the test, the parameter of the modules were $R_1 = R_2 = 1 \Omega$, $C_1 = C_2 = 6$ mF, $L_1 = L_2 = 6.6$ mH, $V_1 = V_2 = 40$ V ac. The dc link output voltage was

$$V_{c1} (= 115) + V_{c2} (= 115) = 230 \text{ V dc.}$$

Power Reversal Test

An experimental test of step power reversal from inverter operation ($i_2 = -5$ A dc) to rectifier operation ($i_2 = +5$ A dc) was successfully performed and is shown in Fig. 12. This provides experimental evidence of stable operation in both the inverter and rectifier modes of operation while maintaining a total dc link voltage of 230 V dc.

PARALLEL-CONNECTED TYPE B

The parallel-connected Type B configuration of Fig. 13 was tested successfully using two rectifier units.

Reversal of Power Test

The photograph in Fig. 14 shows the oscillograms of the three-phase currents in slave unit as a step change of the output dc link current i_2 from -10 A dc (inverter) to $+10$ A dc (rectifier) is demanded. It is established that stable inverter and rectifier regimes exist for parallel configuration. From the oscillogram one sees that the currents have good sinusoidal waveforms although there is slight distortion.

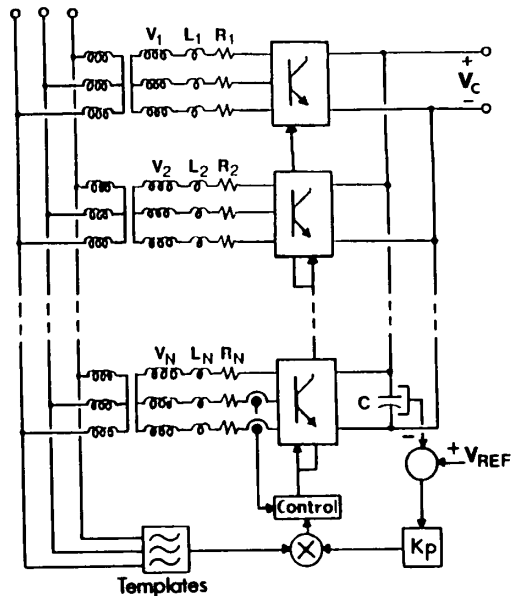


Fig. 13. Parallel-connected Type B.

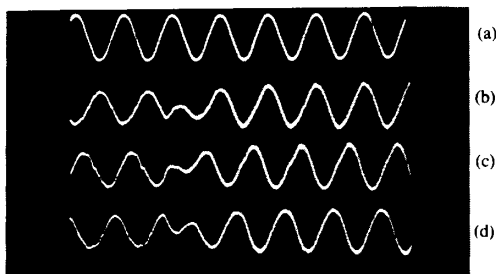


Fig. 14. Parallel-connected Type B during step reversal from inverter to rectifier operation. Slave waveforms: (a) Phase-a voltage, 40 V rms. (b) Phase-b current from 4.5 to 6 A rms. (c) Phase-b current from 4.5 to 6 A rms. (d) Phase-c current from 4.5 to 6 A rms.

Sensitivity to Component Tolerances

A critical issue to the success of the Type-B configuration is whether the good sinusoidal current waveforms will be maintained if the transformers, resistances, inductances, and capacitances have the usual engineering tolerances. Several digital simulations involving a master and three slaves with scattered variations of the parameters show that the waveform distortion is not a serious issue.

It is found that the ac phase inductance affects the sharing of current in parallel connections and the sharing of voltage in series connections. For example, a ± 5 -percent deviation in L_n results in

$$\text{parallel connection} \approx 5\% \text{ in } I_n, 5\% \text{ in } i_{1n}$$

$$\text{series connection} \approx 10\% \text{ in } I_n, 10\% \text{ in } V_{cn}.$$

Comparison of Systems

Table I summarizes the component count of the two configurations under study.

TABLE I

Type	Connection	Current Sensors	Voltage Sensors	Multipliers and Controls
A	Series	$2N$	N	N
	Parallel	$2N$	1	N
B	Series	2	1	1
	Parallel	2	1	1

CONCLUSION

The study shows that Type B, while being by far more economical than Type A, does not suffer unduly from deficient performance. Further investigation is needed to evaluate the full possibilities of Type B. Meanwhile, Type A is a sure and certain standby until the expectations for Type B are fully confirmed.

ACKNOWLEDGMENT

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