

# AN ACTIVE POWER FILTER IMPLEMENTED WITH A THREE-LEVEL NPC VOLTAGE-SOURCE INVERTER

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**Abstract.** This paper presents an active power filter implemented with a three-level neutral point-clamped voltage-source inverter. The active power filter can compensate current harmonics and reactive power in medium voltage distribution systems. The paper presents the principles of operation and design criteria for both the power and control circuits. Finally, the viability of the proposed scheme is shown with computer simulation using Matlab.

## I.- INTRODUCTION

Active power filters are expected to play an important role in reducing harmonic contamination in power distribution systems [1]-[3]. So far shunt active power filters implemented with two levels PWM voltage-source inverters have been researched and proposed in the technical literature [1]-[2]. Many of these equipment are already been used to compensate power factor and current harmonics in power distribution systems [1]. Due to the power handling capabilities of actual power semiconductor devices these types of active power filters are connected through a coupling transformer to match with the source voltage. In order to achieve higher power level, voltage source inverters are connected in parallel to the dc bus [2]. This type of connection requires a transformer with multiple secondary windings, increasing the cost and complexity of the power topology. The series connection of several semiconductors controlled in synchronism to obtain an equivalent high voltage switch presents serious voltage sharing problems. In this type of topology the static and dynamic sharing of the voltage across each switch is quite difficult. Moreover, since all the switches must commutate at the same time, the generated  $dv/dt$  by each commutation produces significant amount of noise, which can affect the surrounding low-voltage control circuits. Also, series active power filter operating with shunt passive filters have been proposed to compensate line current harmonics [2]. Series

compensation requires low power PWM voltage-source inverters to generate the harmonic voltage components necessary to isolate the respective current harmonics from the power source. Although series active power filters present excellent current harmonics compensation, their main disadvantage is related with the protection scheme which has limited their applications in power distribution systems.

In recent years, there has been an increasing interest in using multilevel inverters for high power energy conversion, specially for drives and reactive power compensation [4]-[8]. Multilevel PWM inverters can be connected to high voltage source without a coupling transformer. The use of neutral-point-clamped (NPC) inverters allows equal voltage shearing of the series connected devices in each phase. However, the neutral point potential deviates, resulting in an excess voltage stress to either the upper or lower set of devices [5].

This paper presents an active power filter implemented with a three-level NPC voltage-source inverter. A new control scheme is developed to follow the current reference signal and to minimize the neutral point potential deviation. The proposed current control method is simple to implement and reduces switching frequency, as compared with other carrier PWM techniques. The instantaneous reactive power concept is used to obtain the inverter current reference signals required to compensate current harmonics and reactive power.

## II.- PRINCIPLES OF OPERATION

Basically, multilevel inverters have been developed for applications in high voltage ac motor drives and static var compensation. For these types of applications, the output voltage of the multilevel inverter must be able to generate an almost sinusoidal output current. In order to generate a near sinusoidal output current, the output voltage should not contain low frequency harmonic components. The generation of the inverter output

voltage is performed by using well known PWM or vector control techniques which will calculate the gating signals.

For active power filter applications the three level NPC inverter output voltage must be able to generate an output current that follows the respective reference current which contain the harmonic and reactive component required by the load. The power circuit topology presented in this paper is shown in Fig. 1. The three level NPC voltage-source inverter is connected in parallel through a link reactor to the power distribution system.

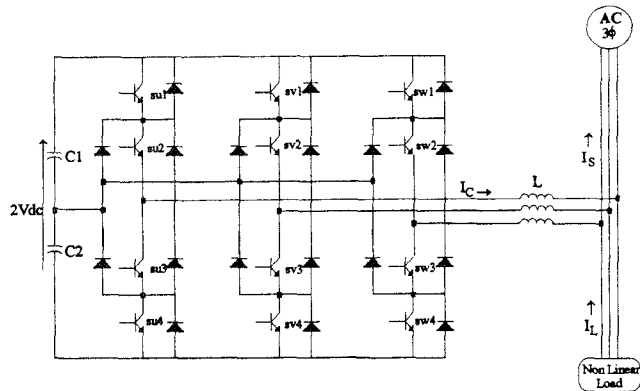


Fig. 1. The active power filter power circuit topology.

The active power filter control scheme uses a vector control to generate the inverter gating signals and is programmed in a DSP. The block diagram of the proposed control scheme is shown in Fig. 2 and consists of a current reference generator, a dc voltage control and the inverter gating signals generator.

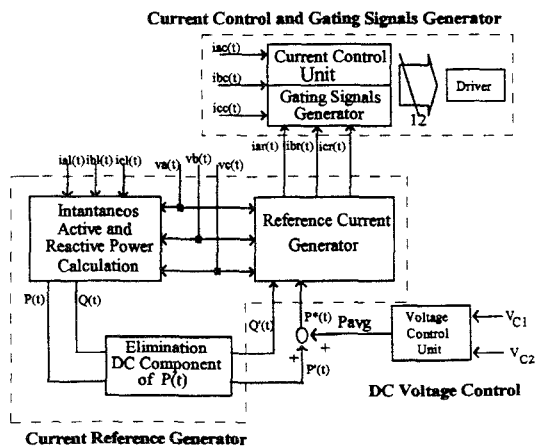


Fig. 2. The block diagram of the proposed active power filter control scheme.

The principles of operation and most important characteristics of each module are described as follows.

### 2.1.- Current Reference Generator

The current reference circuit generates the reference currents required to compensate the load current harmonics and reactive power, and also to maintain constant the dc voltage across the two electrolytic capacitors. The reference currents are obtained by using the instantaneous reactive power concept introduced by Akagi in [2]. The values of the reference currents are obtained by using the following expression:

$$\begin{bmatrix} i_{a\_ref} \\ i_{b\_ref} \\ i_{c\_ref} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \times \begin{bmatrix} v_{\alpha} & v_{\beta} \\ -v_{\beta} & v_{\alpha} \end{bmatrix}^{-1} \times \begin{bmatrix} p' \\ q' \end{bmatrix} \quad (1)$$

where  $p'$  is the ac component of the instantaneous active power and  $q'$  is the instantaneous reactive power associated with the non linear load. The active power required to maintain the dc voltage constant depends on the amplitude of the reference currents. In order to keep the dc voltage under control it is necessary to modified the amplitude of the inverter reference current. This is done by the dc voltage control unit.

### 2.2.- Current control circuit.

The compensation effectiveness of an active power filter depends on its ability to follow with a minimum error and time delay the reference signal. The scheme proposed in this paper uses a vector control technique to generate the inverter gating signals. The vector control circuits selects the next combination of semiconductors that will reduce the current error forcing the inverter output current to follow the reference signal closely.

The state equation of the active power filter is equal to:

$$L \frac{d\Delta i}{dt} = E - V(k) \quad (2)$$

where  $E$  represents the source instantaneous line voltage and  $V(k)$  the inverter output voltage. This equation shows that in order to keep the current error  $\Delta i$  close to zero, the source vector voltage,  $E$ , must be close to the inverter vector output voltage  $V(k)$ . The selection of the next  $V(k)$  is done by evaluating the following expression:

$$\Delta i - E - V(k) = 0 \quad (3)$$

Each time  $\Delta i$  is higher than a predefined value, the control scheme selects the combination of switches that satisfies equation (3).

The space vector representation of the three level inverter output voltage  $V(k)$  is shown in Fig. 3.

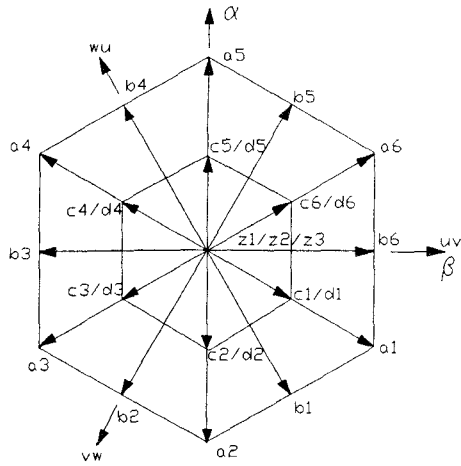


Fig. 3. The space vector representation of the three level inverter output voltage.

The classification of the different vector voltages  $V(k)$  is shown in Table I [8].

Table I.  
Classification of the inverter output voltage vectors

Output voltage vector $V(k)$				
Group	n	condition	n	condition
a	1	P+P-P-	2	P+P+P-
	3	P-P+P-	4	P-P+P+
	5	P-P-P+	6	P+P-P+
b	1	P+OP-	2	OP+P-
	3	P-P+O	4	P-OP+
	5	OP-P+	6	P+P-O
c	1	P+OO	2	P+P+O
	3	OP+O	4	OP+P+
	5	OOP+	6	P+OP+
d	1	OP-P-	2	OOP-
	3	P-OP-	4	P-OO
	5	P-P-O	6	OP-O
z	P+P+P+ OOP-P-P-			

According with the amplitude, the inverter output voltage vectors  $V(k)$  are classified in 5 different groups [8]. Each group defines which capacitor is connected to the ac lines. When the inverter is operating with an output voltage that belongs to group *a* or *b*, it means that the two capacitors are connected to the ac lines. When the voltage is in group *c* the top capacitor  $C1$  is connected and if the voltage is in group *d* the bottom capacitor  $C2$  is connected to the ac lines. In Table I, P+ represents the condition when the positive dc bus (P+) is connected to the ac source, P- means that the negative dc bus is connected to one of the ac lines and finally, 0 means that the neutral point of the dc bus (NP, between the two dc

capacitors) is connected to the ac source. For example, when the inverter output voltage vector is equal to  $a1$ , P+ is connected to phase a, P- is connected to phase b and c, and the amplitude of the line to line inverter output voltage is  $2 V_{dc}$ .

If P+ needs to be connected to one of the three ac lines, the two upper switches must be turned on, and the two lower switches must be turned off. On the other hand, if P- needs to be connected to the ac lines, the two lower switches must be turned on and the two upper switches must be turned off. Finally, if the neutral point, NP, needs to be connected to the ac side, the two central switches must be turned on and the two external switches must be turned off. These three operating modes are shown in Fig. 4.

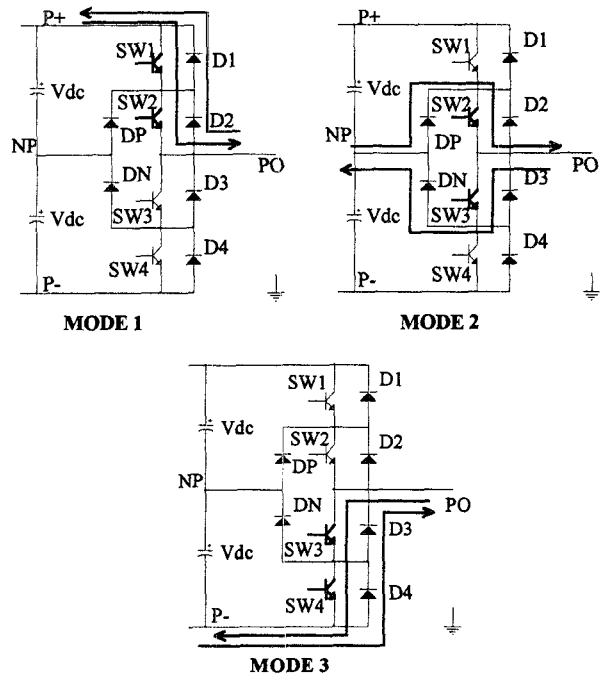


Fig. 4. The three modes of operation of a three level NPC voltage source inverter.

In **Mode 1** switches 1 and 2 are conducting, and  $+V_{dc}$  is reflected to the ac side. When the current is positive, it flows through  $Sw1$  and  $Sw2$ , while if it is negative it is conducted by the diodes  $D1$  and  $D2$ .

In **Mode 2**, switches 2 and 3 are conducting. In this case the neutral point is connected to the ac side, which means that the inverter output voltage is zero. The positive line current circulates through  $DP$  and  $Sw2$ , while the negative current flows through  $Sw3$  and  $DN$ .

Finally, in **Mode 3** the switches  $Sw3$  and  $Sw4$  are turned on. The positive current flows through  $D4$  and  $D3$ , while the negative current circulates through  $Sw3$  and  $Sw4$ . The inverter output voltage is  $-V_{dc}$ .

### 2.3.- DC Voltage Control Scheme.

The dc voltage control unit must keep the total dc bus voltage constant and equals to a given reference value, and also it must keep the voltages across the two capacitors equals and balanced. The dc voltage control is achieved by adjusting the small amount of real power absorbed by the three level inverter. This small amount of real power is adjusted by changing the amplitude of the fundamental component of the reference current (Fig. 2).

One of the most important feature of the dc voltage control scheme is to keep the voltage across the two capacitors balanced and equals to a given reference. If the two voltages are different, the blocking voltage of the upper and lower controlled switches are not equals. Voltage unbalance is generated if an average current flows between the dc bus neutral point, NP, and the ac lines. The voltage control across each capacitor is done independently.

The dc voltage control unit has two modes of operation:

- i) If the total dc bus voltage needs to be adjusted.
- ii) If only one of the voltage capacitor presents and error larger than a predefined value.

If the total voltage across the dc bus needs to be modified to follow the reference value, any of the 27 switching combinations shown in Fig. 3 can be applied to the voltage source inverter. On the other hand, if it is necessary to change the voltage across the upper or lower capacitor, then the control scheme must select the switching combination that allows to charge or discharge the given capacitor.

The block diagram of the proposed dc voltage control scheme is shown in Fig. 5.

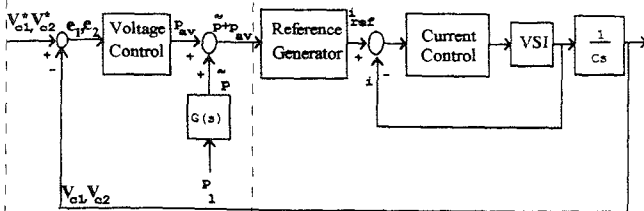


Fig. 5. The block diagram of the proposed dc voltage control scheme.

### 2.4.- Gating Signals Generator

The gating signals generator and the current control units play an important role in active power filters since they define the converter switching frequency, the converter time response and the accuracy to follow the current references. Also, for high power applications it is important to operate with a low switching frequency and

high voltage gain. The gating signals defined by the current control unit try to minimize the magnitude of the current error. The selection of the inverter output voltage is done by evaluating equation (3).

For example, if the vector source voltage  $E$ , and the current error voltage  $\Delta i$  are located as shown in Fig. 6 (a) and (b), then the optimum inverter output voltage is  $c5/d5$ , since the resultant vector  $E - c5/d5$  ( $P1$ ) minimizes the current error  $\Delta i$ . In order to decide which one to select ( $c5$  or  $d5$ ), the control scheme evaluates the magnitude of the dc voltage error and the sense of the current flowing through each of the dc capacitors. If  $C1$  presents a dc voltage higher than its reference value, and  $c5$  generates a dc current that will discharge  $C1$ , then this voltage state is selected.  $d5$  will modify the voltage across  $C2$ .

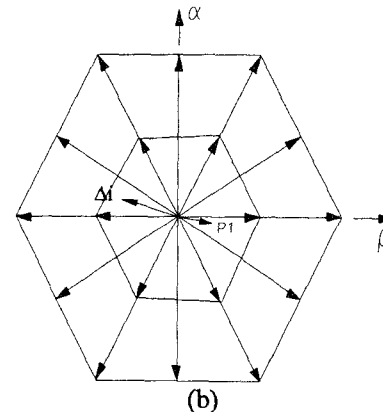
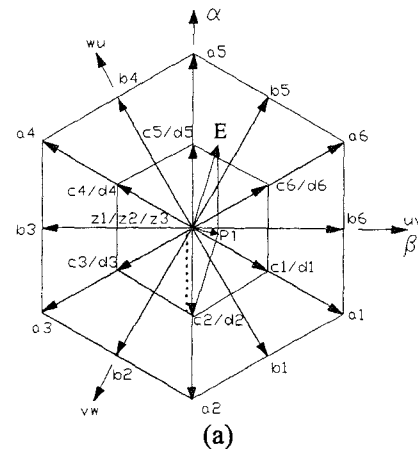


Fig. 6. Example of the selection of the inverter output vector voltage.

## III.- POWER CIRCUIT DESIGN

The principal components of the active power filter topology are the three link reactors and the two dc capacitors. The values of the link reactor and dc capacitor define the transient time response of the three level inverter. The link reactor must allow the  $di/dt$  at the

inverter output current required to follow the reference waveform imposed by the control system. The dc capacitors must be able to keep the dc voltage constant under transient operating conditions resulting from fast changes in the load. Transient changes in the dc bus voltage are also compensated by the voltage control scheme.

*i) Link Reactor*

The maximum slope of the inverter output current may be obtained from equation (4). The evolution of the inverter output current is shown in Fig. 7. From this figure, the slope of the inverter output current is equal to:

$$\frac{\Delta i}{\Delta t} = \frac{2\delta}{1/2f_c} \quad (4)$$

The voltage drop across the link reactor is equal to:

$$L \frac{di}{dt} = V(k) - E \quad (5)$$

By replacing (4) in (5), the value of L is obtained:

$$L = \frac{V(k) - E}{4.\delta.f_c} \quad (6)$$

where V(k) is the inverter output voltage, E the instantaneous voltage of the ac source,  $\delta$  the amplitude of the error current and  $f_c$  the maximum switching frequency.

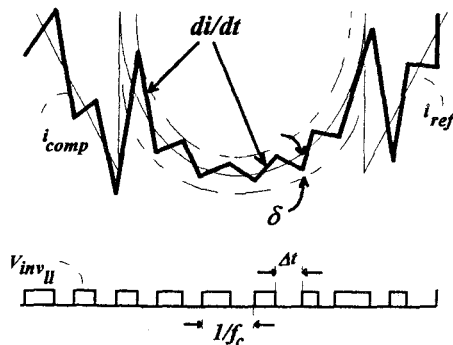


Fig. 7. The evolution of the inverter output current as a function of time.

*ii) Dc Capacitor*

One of the selection criteria used to calculate the value of C1 and C2, is related with the maximum voltage fluctuation allowed in the dc bus when transient changes in the load occur. In this case, the value of the two capacitors is obtained from the following equation:

$$C = \frac{1}{\Delta V} \int_{t_1}^{t_2} i_c(t) dt \quad (7)$$

where  $i_c$  is the instantaneous current flowing through each dc capacitors, and  $\Delta V$  the voltage fluctuation of the dc bus.

**IV.- SIMULATED RESULTS**

The viability of the proposed active power filter topology was proved by computer simulation using Matlab. The active power filter control technique was proved by compensating the reactive power and current harmonic components generated by a six pulses controlled rectifier. Simulated current and voltages waveforms for steady state operating conditions are shown in figures 8 to 12.

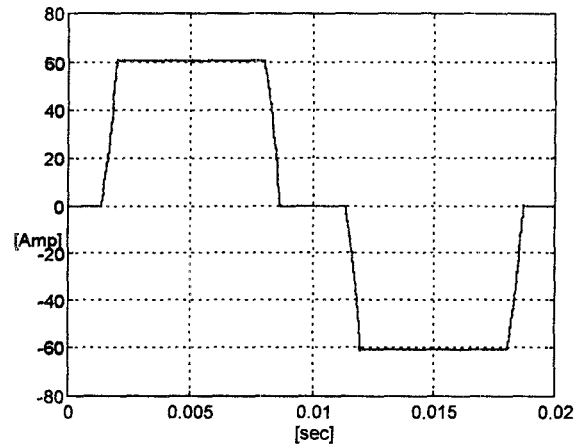


Fig. 8. Simulated current waveform of the non linear load.

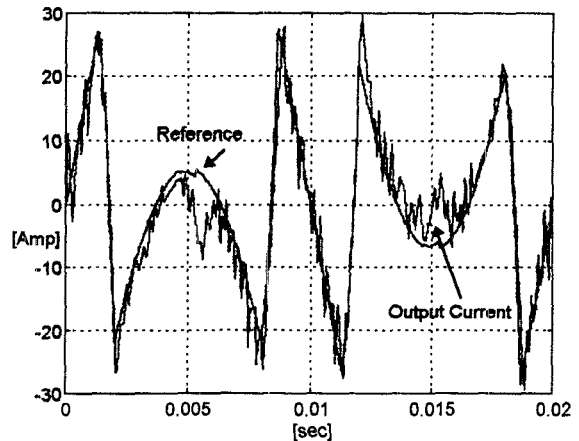


Fig. 9. The current reference signal of the active power filter and the corresponding inverter output current.

## V.- CONCLUSION

An active power filter implemented with a three level neutral point clamped voltage source inverter has been presented and analyzed in this paper. The active power filter uses the instantaneous reactive power concept to calculate the current reference signals. The vector control technique was used to generate the inverter gating signals. The technical viability of the proposed scheme was proved by simulation using Matlab.

## ACKNOWLEDGMENT

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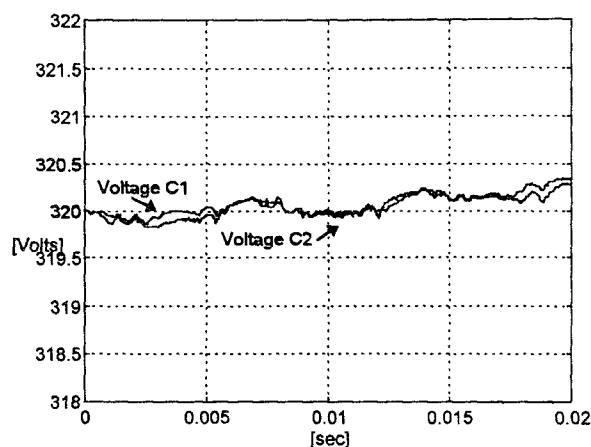


Fig. 10. The dc voltage across capacitors C1 and C2.

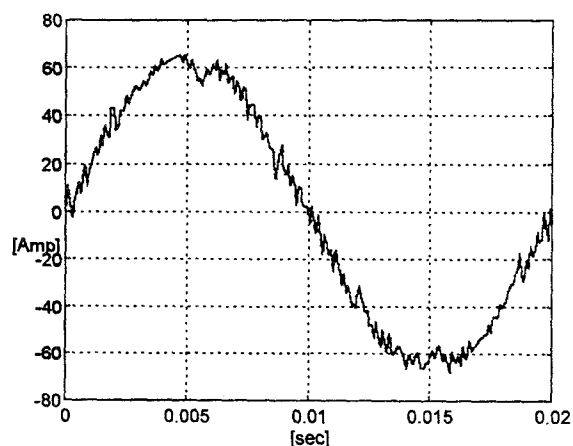


Fig. 11. The ac source compensated current.

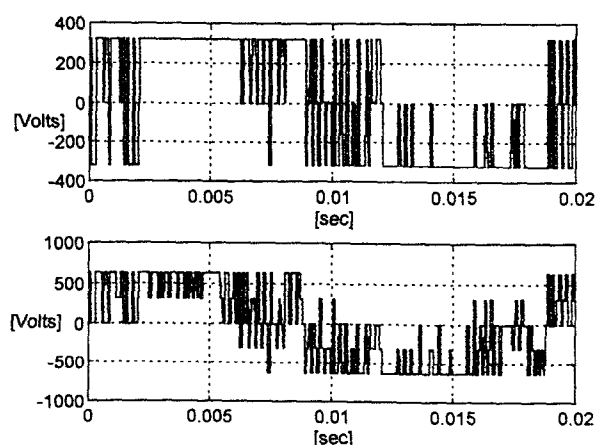


Fig. 12. The inverter output phase and line to line voltage.

The simulated current and voltage waveforms proved the feasibility of the proposed active power filter. The simulated results were obtained with a switching frequency equals to 10 kHz.