

A SIMPLE AND LOW COST CONTROL STRATEGY FOR ACTIVE POWER FILTERS CONNECTED IN CASCADE

Luis Morán* Luciano Fernández* Juan Dixon** Rogel Wallace*

* Dept. of Electrical Engg.
Universidad de Concepción
P.O. Box 53-C
Concepción - CHILE
Fax: 56-41-240280
Email: l Moran@mozart.die.udec.cl

** Dept. of Electrical Engg.
Universidad Católica de Chile
P.O. Box 306 Correo 22
Santiago - Chile
Fax: 56-2-5524054
Email: jdixon@ing.puc.cl

ABSTRACT.- *A simple and low cost control strategy for active power filters implemented with PWM voltage-source inverters connected in cascade is presented and analyzed in this paper. The principal component of the control circuit is an INTEL 8031 AH microcontroller, which generates the current reference waveforms for each converter and the respective switching patterns. The switching pattern is obtained by using a vector control technique. The proposed active power filter consists of two PWM voltage-source inverter connected in cascade each one operating at different switching frequency.*

In particular this paper presents the proposed control strategy in terms of principles of operation, circuit design and implementation. Finally key predicted results are verified experimentally on a 10 kVA bread board model.

I.- INTRODUCTION

The wide-spread application of nonlinear loads is leading to a significant degradation in the power quality offers by supply networks. The users achieve energy efficiency at the expense of generating current harmonics [1]. The presence of current and voltage harmonics in power distribution systems generates more losses in the lines, decreases the power factor and can produce resonance with capacitors connected in parallel to the system. Also, precision instruments, communication equipment and control systems may be affected by the EMI associated with high frequency current harmonics [2]. Therefore, utility power quality has become an important issue for both utilities and their customers.

To alleviate harmonic related problems, several power distribution utilities are starting to impose more severe standards to their customers. These standards limit the amplitude of the current harmonic components that can be generated by the customers and also limit the maximum total harmonic distortion of the voltage waveform that can be supplied by the utility. The application of these stan-

dards has increased the need for more efficient and reliable approaches for harmonic filtering techniques [3].

Traditionally, passive filters have been used to absorb current harmonics generated by high power non-linear loads. However, it is well known that the compensation characteristic of passive filters is influenced by the power system equivalent impedance and also, they are susceptible to generate parallel or series resonance with the power supply. In the last decade, active power filters have been researched and developed to suppress harmonics generated by static power converters and large capacity power apparatus [4]. Different active power filter configurations using series and shunt connection have been proposed, and are gradually being recognized as a viable solution to the problems created by harmonic components [5]. Although series active power filters present advantages in terms of reduced rated power capacity and filtering characteristics, their main disadvantage is that they are difficult to protect against power system faults, and the achievement of power factor compensation is not easy [6]. Moreover, in order to operate properly, it is necessary to connect a passive LC filter between the load and the series active power filter. On the other hand, active power filters connected in parallel are independent of power distribution faults, so that protection scheme can be easily implemented, and with these topologies the power factor as well as current harmonic compensation can be easily implemented [5].

A simple and low cost control strategy for a three-phase active power filter implemented with two PWM voltage-source inverters connected in cascade is presented and analyzed in this paper. The two active power filters are connected in parallel to the system and can compensate the reactive power and the harmonic current components of a nonlinear load. By using two PWM voltage-source inverters in cascade, the compensation characteristics of the active power filter are significantly improved. Each PWM voltage-source inverter uses a vector control technique to generate the required switching pattern.

The topology of the three-phase active power filter presented in this paper is shown in Fig. 1. The voltage-source inverter connected closer to the nonlinear load compensates the displacement power factor and the low frequency current components required by the nonlinear load, while the second inverter compensates only the high frequency current components.

Although there are a number of articles which deal with the analysis of active power filters using force-commutated voltage-source inverters connected in parallel [7] - [11], the three-phase active power filter proposed in this paper differs from previously discussed approaches in the following ways:

- a) Each PWM voltage-source inverter operates with different switching frequency allowing the generation of specific current harmonic components of the load. In that way, the converter connected closer to the load operates at lower switching frequency (400 Hz) and compensates the reactive power and the low frequency current components required by the load. The second inverter operates at higher switching frequency and compensates the current harmonic components that can not be generated by the first converter.
- b) Since the converter connected closer to the load will generate a higher rms current and will operate at lower switching frequency, it can be implemented with GTO's or fast thyristors, which can stand larger rms currents. The second inverter can be implemented with bipolar transistors or IGBT's since it will operate at higher switching frequency but will generate a lower rms current.
- c) By connecting the two inverters in cascade a significant improvement in the active power filter compensation characteristics is achieved since the second inverter will generate all the current harmonic that the first converter is not able to provide.

Moreover, compared with active power filters using quad series PWM inverters [8]-[9], the proposed topology requires less number of converters, a conventional transformer, and a simpler control circuit. Compared with active power filters implemented with parallel converters [10], the active power filter proposed in this paper presents a better compensation performance since, the second converter compensates the current harmonics introduced by the low frequency PWM techniques used in the first converter. Also, since the control system of both converter are completely independent, the overall active power filter compensation characteristic is improved.

The treatment presented in this paper includes the principles of operation and control system design and implementation. Finally, the validity of the proposed control scheme is confirmed experimentally on 10 kVA bread board unit.

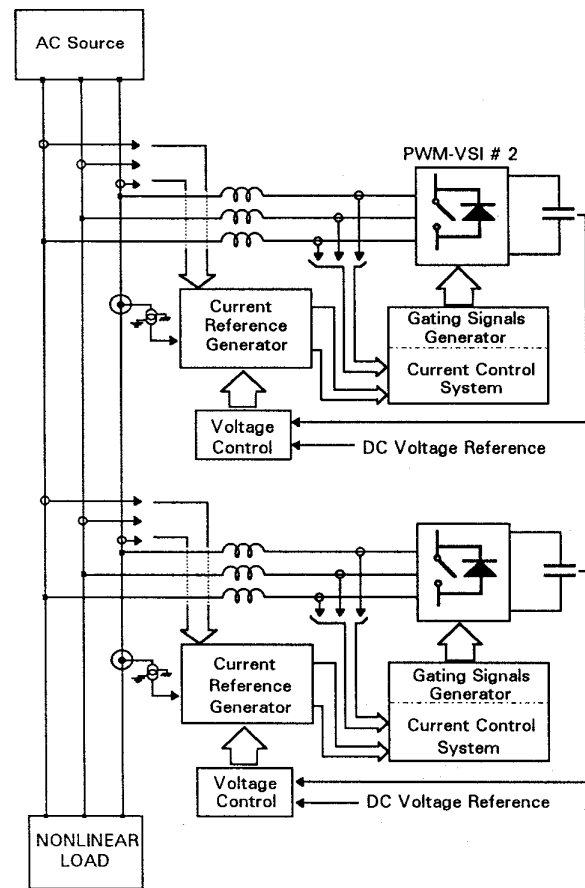


Fig. 1. The proposed active power filter configuration.

II.- PRINCIPLES OF OPERATION

Since active power filters compensates current harmonic components by injecting equal-but-opposite current harmonic components at a specific point of a power system, the compensation characteristic depends mainly on the control strategy. The control scheme of each PWM inverter has to be able to obtain the current reference waveform for each phase of the inverter, maintain the dc voltage constant, and has to generate the inverter gating signals. The block diagram of the proposed control scheme of each converter is shown in Fig. 2.

The current reference signals required by each converter are obtained by using the Instantaneous Reactive Power Concept [6]. Current control is achieved by using the vector control technique proposed in [11]. This control scheme divides the α - β reference frame of the voltage and current in six regions, phase-shifted by 30 degrees, as shown in Fig. 3.

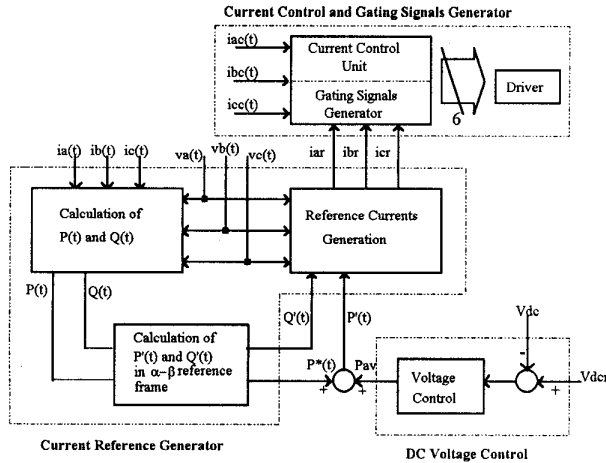


Fig. 2. The block diagram of each PWM-VSI control scheme.

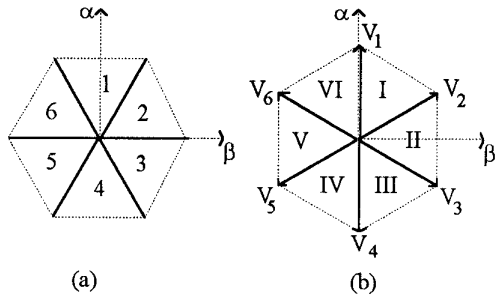


Fig. 3. The hexagons defined by the control scheme. a) The hexagon defined by the inverter output current vector. (b) The hexagon defined by the inverter output voltage vector.

The control system identifies the region where the current error vector is located and selects the inverter output voltage that will force the current error to change in the opposite direction, keeping the inverter ac current closer to the reference signal. Applying Kirchhoff law at the output of the inverter, the following equations are derived (Fig. 1):

$$V(k) = L \frac{di_{gen}}{dt} + E_0 \quad (1)$$

where $V(k)$ is the inverter output voltage, E_0 is the phase to neutral source voltage, L is the synchronous inductor, and i_{gen} is the inverter output current. The current error Δi is defined by:

$$\Delta i = i^* - i_{gen} \quad (2)$$

By replacing (1) in (2) and defining a fictitious vector voltage "E" equals to $Ldi^*/dt + E_0$ then the following equation is obtained:

$$L \frac{d\Delta i}{dt} = E - V(k) \quad (3)$$

Equation (3) represents the active power filter state equation and shows that the current vector error variation $d\Delta i/dt$, is defined by the difference between the fictitious vector voltage E and the inverter output voltage $V(k)$. In order to keep $d\Delta i/dt$ close to zero $V(k)$ must be selected near E . By selecting the inverter output voltage that presents the largest opposite direction component to the current error a faster time response in the current control loop is achieved. The selection of the inverters switching mode can be explained considering that the voltage E is located in Region I (Fig. 3-a) and the current error vector Δi is in Region 6 (Fig. 3-b). The inverter voltage vectors located closer to E are V_1 and V_2 . The vectors $E-V_2$ and $E-V_1$ define two vectors $Ld\Delta i/dt$, located in region III and IV respectively, so in order to reduce the current vector error Δi , $Ld\Delta i/dt$ must be located in Region III, thus the inverter output voltage has to be equal to V_1 . By doing the same analysis for all the possible combinations, the inverter switching modes for each location of Δi and E can be defined (Table I).

Table I
Inverter Switching Modes

E Region	Δi Region					
	1	2	3	4	5	6
I	V_1	V_2	V_2	V_0-V_7	V_0-V_7	V_1
II	V_2	V_2	V_3	V_3	V_0-V_7	V_0-V_7
III	V_0-V_7	V_3	V_3	V_4	V_4	V_0-V_7
IV	V_0-V_7	V_0-V_7	V_4	V_4	V_5	V_5
V	V_6	V_0-V_7	V_0-V_7	V_5	V_5	V_6
VI	V_1	V_1	V_0-V_7	V_0-V_7	V_6	V_6

If the current error vector Δi exceeds a defined amplitude a better combination of vector voltage $E-V(k)$ can be obtained in order to reduce the magnitude of the current error faster. The new value of $V(k)$ is selected only if the current error amplitude is higher than a predefined value h . In this case the best inverter output voltage $V(k)$ correspond to the value located in the same region of Δi .

The inverter switching modes characteristic are defined depending on the amplitude of the current error. If Δi is smaller than δ no commutation is applied to the inverter. If the amplitude of Δi is between δ and h , the switching mode shown in Table I must be applied. Finally, if Δi is larger than h , the inverter output voltage that is selected correspond to the one located in same region than Δi . Switching frequency may be fixed by controlling the time between commutation and by not applying a new switching pattern if the time between two successive commutation is lower

than a selected value. Figure 4 shows the block diagram of the inverter current control scheme.

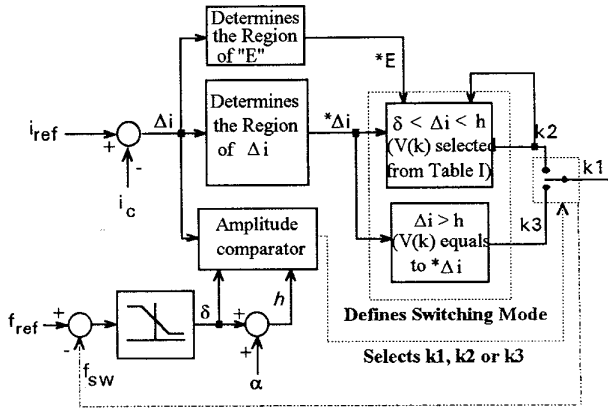


Fig. 4. The current control block diagram.

In Fig. 4 *E represents the Region where the vector E is located, * Δi the Region of Δi , k1 keeps the same value of k (no commutation in the inverter), k2 selects the new inverter output voltage from Table I, and k3 defines V(k) equals to the Region of Δi .

The steady state and transient performance of the proposed current control scheme was proved by computer simulation. The transient behavior of the active power filter was proved for the compensation of a step change in the gating signals of a six pulses controlled rectifier. Simulated waveforms are shown in Fig. 5.

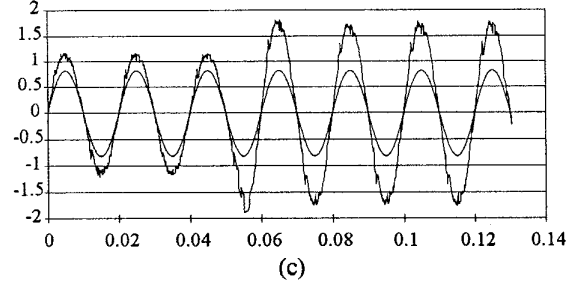
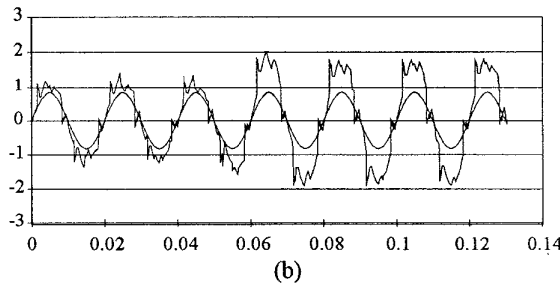
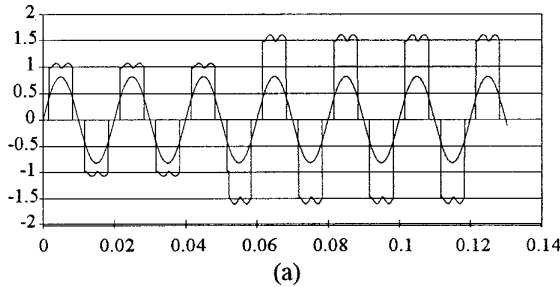


Fig. 5. Simulated results for transient operating conditions. (a) Load current and phase to neutral voltage. (b) Line current between the two converters and phase to neutral voltage. (c) Compensating line current and respective phase to neutral voltage.

III.- ACTIVE POWER FILTER DESIGN

3.1.- Power Circuit Design

The proposed active power filter is implemented with two PWM Voltage-Source inverters connected in parallel to the power system. Each converter has its own control system and sense their own current and voltage signals. The values of the link reactor and dc capacitor define the transient response of each converter. The link reactor must allow the di/dt at the inverter output current required to follow the reference waveform imposed by the control system. The dc capacitor must be able to keep the dc voltage constant under transient operating conditions generates by fast changes in the load equivalent impedance. Transient changes in the dc bus voltage are also compensated by the voltage control scheme.

The value of the link inductor is defined by the following expression:

$$L = \frac{V(k) - E_0}{4.8.f_c} \quad (4)$$

where V(k) is the inverter output voltage, E_0 the instantaneous voltage of the ac source, δ the amplitude of the error current and f_c the maximum switching frequency.

One selection criteria used to calculate the value of C, is related with the maximum voltage fluctuation allowed in the dc bus when transient changes in the load equivalent impedance occurs. In this case, the value of C is obtained from the following equation:

$$C = \frac{1}{\Delta V} \int_{t_1}^{t_2} i_c(t) dt \quad (5)$$

The rated power of each converter is related with the switching frequency. In this case the first inverter operates at 400 Hz and the second at 1.5 kHz. For these switching frequencies and considering a THD in the ac source current lower than 5%, the rated power of each converter with

respect to the load rated power are 26% and 8.7% respectively.

3.2.- Control Circuit Design

The proposed control circuit is implemented with an INTEL 8031 AH microcontroller with 32 KB of memory, 16 KB of EPROM and 16 KB of RAM (Fig. 6). The program stored in the EPROM controls the PWM voltage-source inverter, calculates the reference currents and the gating signals of each converter. The RAM is used to store the data required by the main program. The microcontroller operates at 12 MHz. Ten ADC0820 converters are used to transform analog current and voltages in digital signals. The time required by each A/D converter is 1 μ s. It is important to note that the A/D conversion of the ten signals is done simultaneously. The fundamental component of the active power is obtained through a low pass finite impulse response (FIR) digital filter tuned at 90 Hz. This type of filter does not introduce phase shift between input and output signals. The set points of the active power filter, i.e. switching frequency, ripple current factor, and dc voltage value can be changed by a host computer.

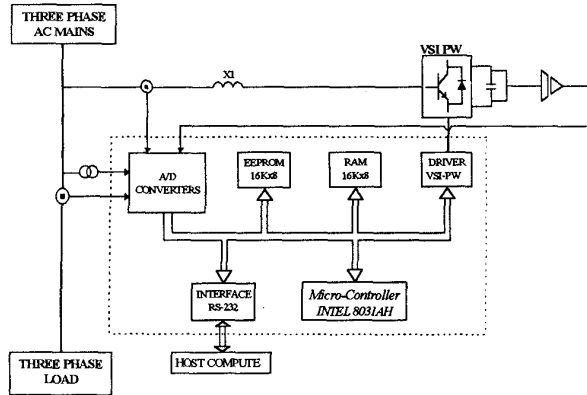


Fig. 6. The proposed control circuit topology for each converter.

The mathematical expression of the FIR digital filter is the following:

$$F(k) = \sum_{i=1}^{\text{order}} h_i \cdot f(k-i) \quad ; k \geq \text{order} \quad (6)$$

where $F(k)$ is the filter output signal and $f(k)$ is the filter input signal. The filter constant h_i were evaluated using the MATLAB software. The constant values are the following:

$$\begin{aligned} h_1 &= h_8 = 0.0088 \\ h_2 &= h_7 = 0.0320 \\ h_3 &= h_6 = 0.1640 \\ h_4 &= h_5 = 0.2793 \end{aligned}$$

The execution time of the filter algorithm is 240 μ s.

Since the INTEL 8031 AH is an 8 bit microcontroller, the multiplication between two 8 bit numbers was done using distributed arithmetic. With this technique the multiplication between two 8 bits variables was reduced to 2 μ s. The block diagram of the programming technique is shown in Fig. 7.

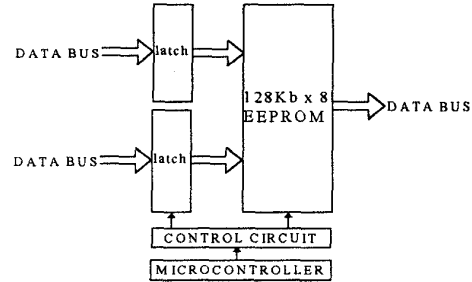


Fig. 7. The block diagram of the programming technique used for the multiplication of two 8 bits variables.

A look-up table was used to multiply a variable with a constant 8 bits number. In this look up table the pointer was using the value of the variable and the offset is made equal to the memory position that will be used in the table.

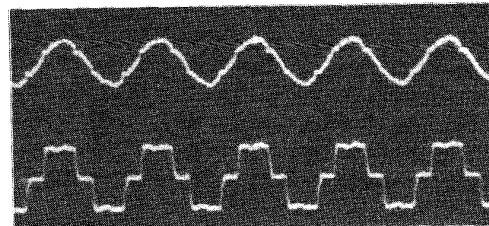
```
movc a, @ a + dptr;
dptr = index of table (in memory address RAM)
a = variable that will be multiplied by a constant
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After the multiplication is done, the accumulator store the result. With this technique, the time required to do a multiplication between a constant and a variable is reduced to 1 μ s.

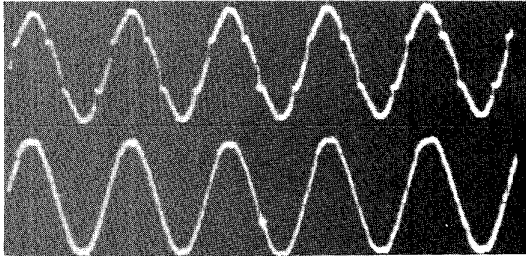
The total execution time of the active power filter control program is 650 μ s.

IV.- EXPERIMENTAL RESULTS

A 10 kVA laboratory prototype using IGBT switches was implemented and successfully tested in compensating a six pulses controlled rectifier. Relevant experimental results obtained with this bread board unit are shown in Figs. 8 and 9.

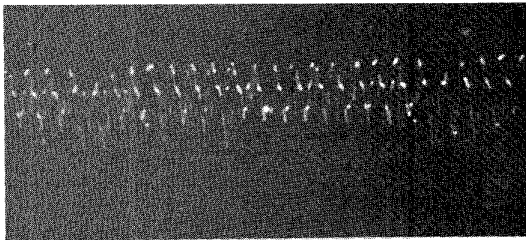


(a)

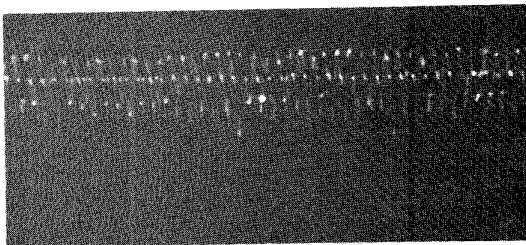


(b)

Fig. 8. Steady-state experimental results. a) The phase to neutral source voltage, 50 V/div, and the respective load current, 5 A/div. b) The phase to neutral source voltage, 50 V/div, and the respective source current, 5 A/div..



(a)



(b)

Fig. 9. Steady-state experimental results. a) The compensating current of inverter # 1. b) The compensating current of inverter # 2.

CONCLUSION

In this paper an active power filter implemented with two PWM voltage-source inverters connected in cascade has been presented and analyzed. The control scheme of each PWM voltage-source inverter is implemented with an INTEL 8031 AH 8 bits microcontroller. Each PWM voltage-source inverter operates at a different switching frequency, allowing the compensation of high power non-linear loads. The closed agreement between the analytical and the experimental results proves the validity of the analysis and the feasibility of the proposed control scheme.

ACKNOWLEDGMENTS

The authors wish to thank the "Fondo de Desarrollo Científico y Tecnológico (FONDECYT)" for the financial support given to the 1940997 project. Also the authors would like to acknowledge the "Dirección de Investigación" of the University of Concepción and the Agency of International Development for the assistance gave through the projects # 20.92.11 and AID # 11.196 respectively.

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