

# A Simple and Low-Cost Control Strategy for Active Power Filters Connected in Cascade

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**Abstract**—A simple and low-cost control strategy for active power filters implemented with pulsewidth modulation voltage-source inverters (PWM-VSI's) connected in cascade is presented and analyzed in this paper. The principal component of the control circuit is an INTEL 8031 AH microcontroller, which generates the current reference waveforms and respective switching patterns for each inverter. The switching pattern is obtained by using a vector control technique. The proposed active power filter consists of two PWM-VSI's, connected in cascade, each one operating at a different switching frequency. This paper presents the proposed control strategy in terms of principles of operation, circuit design, and implementation. Finally, predicted results are verified experimentally on a 10-kVA breadboard model.

## I. INTRODUCTION

THE proliferation of nonlinear loads is resulting in degradation in the power quality of power distribution networks. The users achieve energy efficiency at the expense of generating current harmonics [1]. The presence of current and voltage harmonics in power distribution systems increases losses in the lines, decreases the power factor, and can cause resonance with capacitors connected in parallel with the system. Also, precision instruments, communication equipment, and control systems may be affected by the EMI associated with high-frequency current harmonics [2]. Therefore, utility power quality has become an important issue for both utilities and their customers.

To alleviate harmonic-related problems, power distribution utilities are starting to impose more severe standards on their customers. These standards limit the amplitude of the current harmonic components that can be generated by the customers and also limit the maximum total harmonic distortion of the voltage waveform allowed to be supplied by the utility. The application of these standards has increased the need for more efficient and reliable approaches for harmonic filtering techniques [3].

Traditionally, passive filters have been used to absorb current harmonics generated by high-power nonlinear loads. How-

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ever, it is well known that the compensation characteristics of passive filters is influenced by the power system equivalent impedance and, also, they can generate parallel or series resonance within the utility power supply. In the last decade, active power filters have been developed to suppress harmonics generated by static power converters and large-capacity power apparatus [4]. Different active power filter configurations using series and shunt connections have been proposed and are recognized as viable solutions to the problems created by harmonic components [5]. Although series active power filters present advantages in terms of reduced rated power capacity and filtering characteristics, their main disadvantage is that they are difficult to protect against power system faults, and achieving power-factor compensation is not easy [6]. Moreover, in order to operate properly, it is necessary to connect a passive LC filter between the load and the series active power filter. On the other hand, shunt active power filters are not affected by power distribution faults, so that a protection scheme can be easily implemented and, with shunt active power filters, the compensation of the power factor, as well as current harmonics can be easily implemented [5].

A simple and low-cost control strategy for a three-phase active power filter implemented with two pulsewidth modulation voltage-source inverters (PWM-VSI's) connected in cascade, is presented and analyzed. Two active power filters are connected in parallel to compensate for the reactive power and current harmonics of a nonlinear load. The use of two PWM-VSI's in cascade significantly improves the compensation characteristics of active power filters. Each PWM-VSI uses a vector control technique to generate the required switching pattern.

The topology of the three-phase active power filter presented in this paper is shown in Fig. 1. The voltage-source inverter connected closer to the nonlinear load compensates for the displacement power factor and the low-frequency current components generated by the nonlinear load, while the second inverter compensates for only the high-frequency current components.

Although there are a number of articles which deal with the analysis of active power filters using force-commutated VSI's connected in parallel [7]–[10], the three-phase active power filter proposed in this paper differs from previously discussed approaches in the following ways.

- 1) Each PWM-VSI operates at a different switching frequency, allowing the generation of specific current harmonic components of the load. In that way, the converter

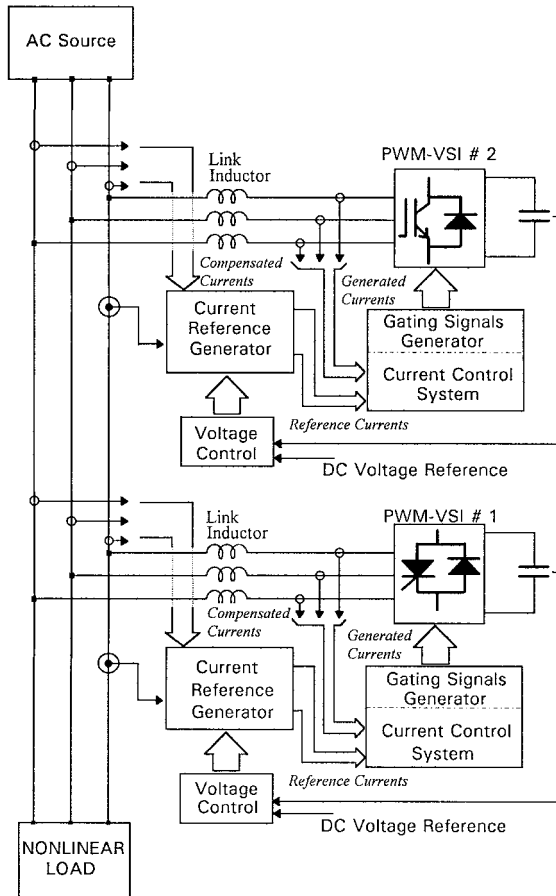


Fig. 1. The proposed active power filter configuration.

connected closer to the load operates at a lower switching frequency (400 Hz) and compensates for the reactive power and the low-frequency current components required by the load. The second inverter operates at a higher switching frequency and compensates for the current harmonic components that cannot be generated by the first converter.

- 2) Since the converter connected closer to the load will generate a higher rms current and will operate at a lower switching frequency, it can be implemented with gate-turn-off switches (GTO's), which can provide larger rms currents. The second inverter can be implemented with bipolar transistors or insulated gate bipolar transistors (IGBT's), since it will operate at a higher switching frequency, but will generate a lower rms current.
- 3) By connecting the two inverters in cascade, a significant improvement in the active power filter compensation characteristics is achieved, since the second inverter will generate all the current harmonics that the first converter is not able to provide.

Moreover, compared with active power filters using quad series PWM inverters [8], [9], the proposed topology requires fewer converters, a conventional transformer, and a simpler control circuit. Compared with active power filters implemented with parallel converters [10], the active power filter proposed in this paper provides better compensation perfor-

mance, since the second converter compensates for the current harmonics introduced by the low-frequency PWM techniques used in the first converter. Also, since the control systems of both converters are completely independent, the overall active power filter compensation characteristic is improved.

The treatment presented in this paper includes the principles of operation, control system design, and implementation. Finally, the validity of the proposed control scheme is confirmed experimentally on a 10-kVA breadboard unit.

## II. PRINCIPLES OF OPERATION

Since shunt active power filters compensate for current harmonic components by injecting equal-but-opposite current harmonic at a specific point of a power system, the compensation characteristic depends mainly on the control strategy. The control scheme of each PWM inverter must calculate the current reference waveform for each phase of the inverter, maintain the dc voltage constant, and generate the inverter gating signals. The block diagram of the proposed control scheme of each converter is shown in Fig. 2.

### A. Current Reference Generator

The current reference signals required by each converter are obtained by using the instantaneous reactive power concept [7]. Depending on the reference signals used, active power filters can compensate for only the system displacement power factor, only current harmonics, or both at the same time. This compensation characteristic is defined by the components of  $p(t)$  and  $q(t)$  used to calculate the inverter reference currents. The instantaneous active and reactive power  $p(t)$  and  $q(t)$  in the  $\alpha$ - $\beta$  reference frame are obtained with the following expressions:

$$p(t) = v_{\alpha}(t)i_{\alpha}(t) + v_{\beta}(t)i_{\beta}(t) \quad (1)$$

$$q(t) = v_{\alpha}(t)i_{\beta}(t) - v_{\beta}(t)i_{\alpha}(t) \quad (2)$$

where  $p(t)$  and  $q(t)$  contain dc and ac components. The dc components are related to the active and reactive power produced by the fundamental components of voltages and currents, while the ac components of  $p(t)$  and  $q(t)$  are associated with the reactive power generated by currents and voltages harmonics. The reference currents  $i_{ar}$ ,  $i_{br}$ , and  $i_{cr}$  are defined by

$$\begin{bmatrix} i_{ar} \\ i_{br} \\ i_{cr} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & 0 \\ -1 & \sqrt{3} \\ -1 & -\sqrt{3} \end{bmatrix} \cdot \frac{1}{v_{\alpha}^2 + v_{\beta}^2} \cdot \begin{bmatrix} -v_{\alpha} & v_{\beta} \\ v_{\beta} & -v_{\alpha} \end{bmatrix} \cdot \begin{bmatrix} p'(t) \\ q(t) \end{bmatrix} \quad (3)$$

where  $p'(t)$  is the ac component of the instantaneous real power.

### B. DC Voltage Control Unit

Fig. 1 shows that each PWM-VSI is connected to a dc capacitor. Voltage control across the dc capacitor is performed

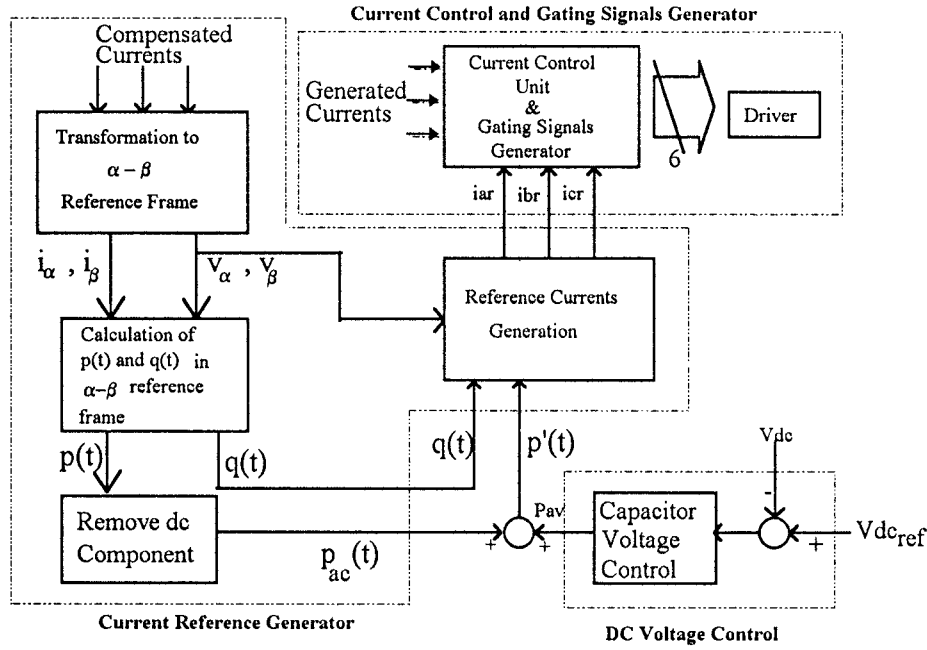


Fig. 2. The block diagram of each PWM-VSI control scheme.

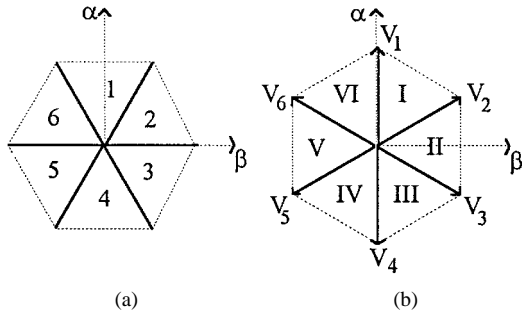


Fig. 3. The hexagons defined in the  $\alpha$ - $\beta$  reference frame by the current control scheme. (a) The hexagon defined by the inverter output current vector. (b) The hexagon defined by the inverter output voltage vector.

by adjusting the small amount of real power absorbed by each converter. This real power depends on the amplitude of the inverter fundamental current component which is in phase with the respective phase-to-neutral voltage. The inverter reference currents contain a small component in phase with the respective phase-to-neutral voltage and with an amplitude proportional to the  $P_{ave}$  signal obtained from the dc voltage control unit (Fig. 2). By adjusting the amplitude of  $P_{ave}$ , each converter will absorb the real power required to cover the switching losses and to maintain the dc capacitor voltage constant.

### C. Gating Signals Generator

The gating signals generator and the current control unit play an important role in active power filters, since they define the converter switching frequency, the converter time response, and the accuracy to follow the current references. Also, for high-power applications, it is important to operate with a constant switching frequency and high voltage gain.

1) *Current Control Scheme:* Current control is achieved by using the vector control technique proposed in [11]. This

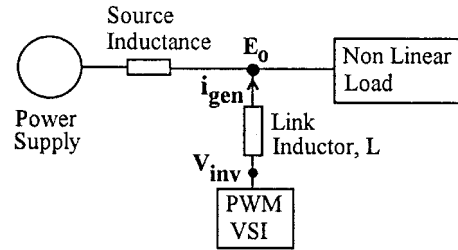


Fig. 4. The single-phase equivalent circuit of one active power filter connected to the power system.

current control technique divides the  $\alpha$ - $\beta$  reference frame of currents and voltages in six regions, phase shifted by  $30^\circ$  (Fig. 3), identifies the region where the current vector error  $\Delta \mathbf{i}$  is located, and selects the inverter output voltage vector  $\mathbf{V}_{inv}$  that will force  $\Delta \mathbf{i}$  to change in the opposite direction, keeping the inverter output current close to the reference signal.

Fig. 4 shows the single-phase equivalent circuit of each active power filter connected to a nonlinear load and to the power supply.

The equation that relates the active power filter currents and voltages is obtained by applying Kirchoff's law to the equivalent circuit shown in Fig. 4:

$$\mathbf{V}_{inv} = L \frac{d\mathbf{i}_{gen}}{dt} + \mathbf{E}_0. \quad (4)$$

The current error vector  $\Delta \mathbf{i}$  is defined by the following expression:

$$\Delta \mathbf{i} = \mathbf{i}_{ref} - \mathbf{i}_{gen} \quad (5)$$

where  $\mathbf{i}_{ref}$  represents the inverter reference current vector defined by (3). By replacing (5) in (4),

$$\begin{aligned} \mathbf{V}_{inv} &= L \frac{d}{dt} (\mathbf{i}_{ref} - \Delta \mathbf{i}) + \mathbf{E}_0 \Rightarrow \\ L \frac{d\Delta \mathbf{i}}{dt} &= L \frac{d\mathbf{i}_{ref}}{dt} + \mathbf{E}_0 - \mathbf{V}_{inv}. \end{aligned} \quad (6)$$

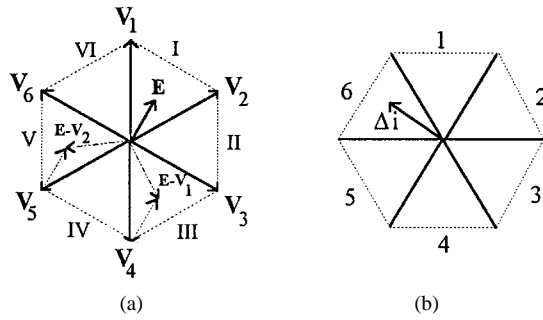


Fig. 5. Selection of the inverter switching pattern according to the region where  $\Delta \mathbf{i}$  and  $\mathbf{E}$  are located. (a) The regions where  $Ld\Delta \mathbf{i}/dt$  are located. (b) The region where  $\Delta \mathbf{i}$  is located.

If  $\mathbf{E} = L(d\mathbf{i}_{\text{ref}}/dt) + \mathbf{E}_o$ , then (6) becomes

$$L \frac{d\Delta \mathbf{i}}{dt} = \mathbf{E} - \mathbf{V}_{\text{inv}}. \quad (7)$$

Equation (7) represents the active power filter state equation and shows that the current error vector variation  $d\Delta \mathbf{i}/dt$  is defined by the difference between the fictitious voltage vector  $\mathbf{E}$  and the inverter output voltage vector  $\mathbf{V}_{\text{inv}}$ . In order to keep  $d\Delta \mathbf{i}/dt$  close to zero,  $\mathbf{V}_{\text{inv}}$  must be selected near  $\mathbf{E}$ . Thus, by selecting the inverter output voltage that provides the largest opposite direction component to the current error, a faster response of the current control loop is achieved.

2) *Selection of the Inverter Switching Mode*: The selection of the inverters' gating signals is defined by the region in which  $\Delta \mathbf{i}$  is located and by its amplitude. In order to improve the current control accuracy and associated time response, depending on the amplitude of  $\Delta \mathbf{i}$ , the following actions are defined.

- If  $\Delta \mathbf{i} \leq \delta$ , the gating signals of the inverter are not changed.
- If  $h \leq \Delta \mathbf{i} \leq \delta$ , the inverter gating signals are defined following *Mode a*.
- If  $\Delta \mathbf{i} > h$ , the inverter gating signals are defined following *Mode b*.

In the above,  $\delta$  and  $h$  are reference values which define the accuracy and hysteresis window of the current control scheme.

*Mode a—Small changes in  $\Delta \mathbf{i}$  ( $h \leq \Delta \mathbf{i} \leq \delta$ ):* The selection of the inverter switching *mode a* can be explained with the following example. Assuming that the voltage vector  $\mathbf{E}$  is located in Region I [Fig. 5(a)] and the current error vector  $\Delta \mathbf{i}$  is in Region 6 [Fig. 5(b)], the inverter voltage vectors  $\mathbf{V}_{\text{inv}}$  located closest to  $\mathbf{E}$  are  $\mathbf{V}_1$  and  $\mathbf{V}_2$ . The vectors  $\mathbf{E}-\mathbf{V}_2$  and  $\mathbf{E}-\mathbf{V}_1$  define two vectors  $Ld\Delta \mathbf{i}/dt$ , located in Regions III and V, respectively, as shown in Fig. 5(a). In order to reduce the current vector error  $\Delta \mathbf{i}$ ,  $Ld\Delta \mathbf{i}/dt$  must be located in Region III, thus, the inverter output voltage has to be equal to  $\mathbf{V}_1$ . In this way,  $\Delta \mathbf{i}$  will be forced to change in the opposite direction, reducing its amplitude faster. By doing the same analysis for all possible combinations, the inverter switching modes for each location of  $\Delta \mathbf{i}$  and  $\mathbf{E}$  can be defined (Table I).  $V_k$  represents the inverter switching functions defined in Table II.

*Mode b—Large changes in  $\Delta \mathbf{i}$  ( $\Delta \mathbf{i} > h$ ):* If  $\Delta \mathbf{i}$  becomes larger than  $h$  in transient state, it is necessary to

TABLE I  
INVERTER SWITCHING MODES

E Region	$\Delta \mathbf{i}$ Region					
	1	2	3	4	5	6
I	$V_1$	$V_2$	$V_2$	$V_0-V_7$	$V_0-V_7$	$V_1$
II	$V_2$	$V_2$	$V_3$	$V_3$	$V_0-V_7$	$V_0-V_7$
III	$V_0-V_7$	$V_3$	$V_3$	$V_4$	$V_4$	$V_0-V_7$
IV	$V_0-V_7$	$V_0-V_7$	$V_4$	$V_4$	$V_5$	$V_5$
V	$V_6$	$V_0-V_7$	$V_0-V_7$	$V_5$	$V_5$	$V_6$
VI	$V_5$	$V_1$	$V_0-V_7$	$V_0-V_7$	$V_6$	$V_6$

TABLE II  
RELATIONSHIP BETWEEN SWITCHING FUNCTION AND INVERTER OUTPUT VOLTAGE

k	Switch on Phase a	Switch on Phase b	Switch on Phase c	Inverter Output Voltage $V_k$
0	4	6	2	0
1	1	6	2	$2/3 V_{dc}$
2	1	3	2	$2/3 V_{dc} e^{j\pi/3}$
3	4	3	2	$2/3 V_{dc} e^{j2\pi/3}$
4	4	3	5	$2/3 V_{dc} e^{j\pi}$
5	4	6	5	$2/3 V_{dc} e^{j4\pi/3}$
6	1	6	5	$2/3 V_{dc} e^{j5\pi/3}$
7	1	3	5	0

choose the switching mode in which the  $d\Delta \mathbf{i}/dt$  has the largest opposite direction to  $\Delta \mathbf{i}$ . In this case, the best inverter output voltage  $\mathbf{V}_{\text{inv}}$  corresponds to the value located in the same region of  $\Delta \mathbf{i}$ .

3) *Switching Frequency Control*: The switching frequency may be fixed by controlling the time between commutations and by not applying a new switching pattern if the time between two successive commutations is lower than a selected value ( $t = 1/2f_c$ ).

Fig. 6 shows the block diagram of the inverter current control scheme which was implemented by software in a microcontroller. In Fig. 6,  $^*\mathbf{E}$  represents the region where the vector  $\mathbf{E}$  is located,  $^*\Delta \mathbf{i}$  the region of  $\Delta \mathbf{i}$ ,  $k_1$  keeps the same value of  $k$  (no commutation in the inverter),  $k_2$  selects the new inverter output voltage from Table I, and  $k_3$  selects  $\mathbf{V}_{\text{inv}}$  in the same region of  $\Delta \mathbf{i}$ .

The steady-state and transient performance of the proposed current control scheme was proved by computer simulation. The transient behavior of the active power filter was simulated for the compensation of a step change in the gating signals of a six-pulse controlled rectifier. Simulated waveforms are shown in Fig. 7.

### III. ACTIVE POWER FILTER DESIGN

#### A. Power Circuit Design

The proposed active power filter is implemented with two PWM-VSI's connected in parallel to the power system. Each converter has its own control scheme and senses its own

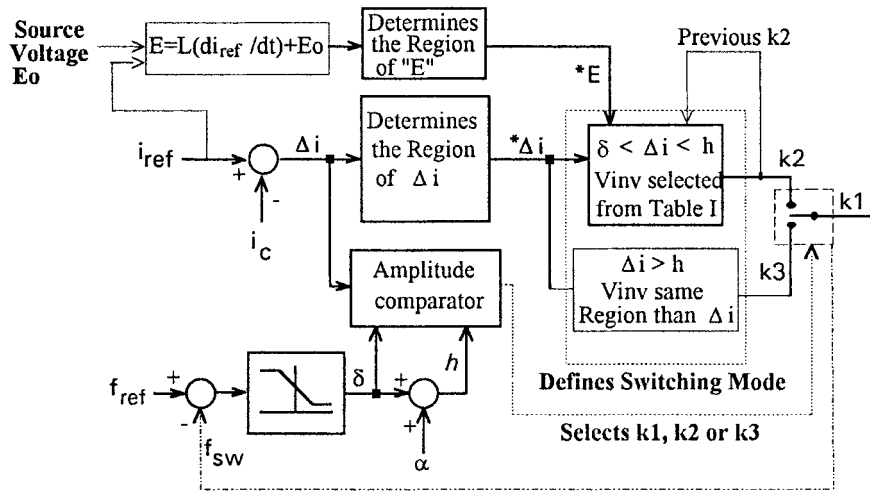


Fig. 6. The current control block diagram.

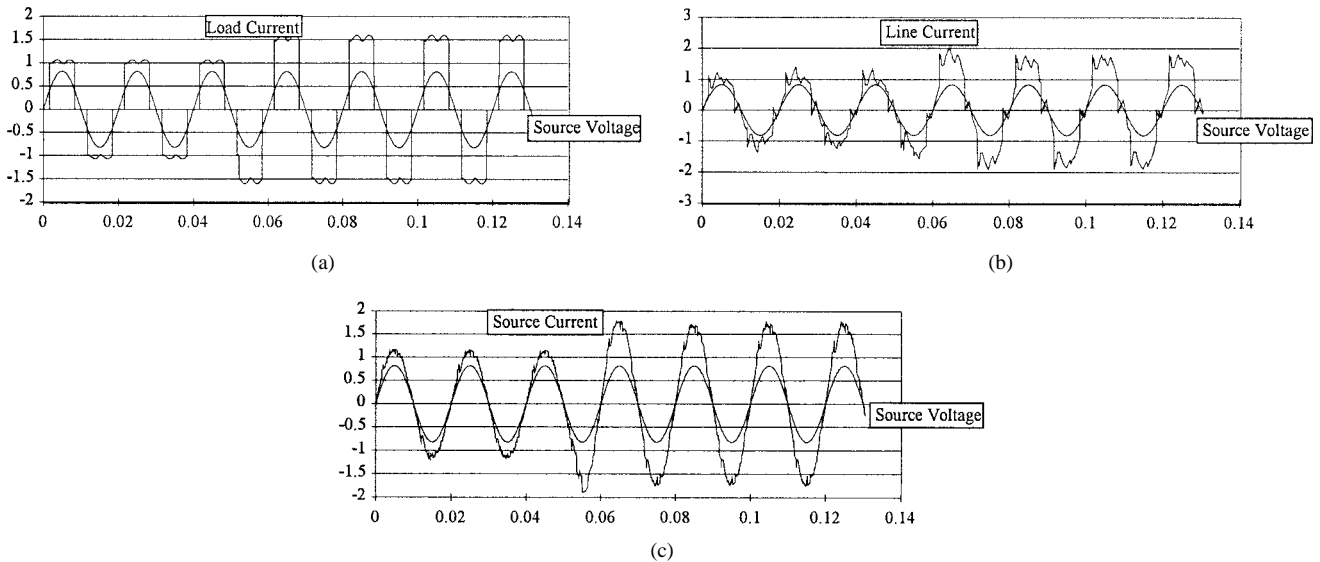


Fig. 7. Simulated results for transient operating conditions. (a) Load current and phase-to-neutral voltage. (b) Line current between the two converters and phase-to-neutral voltage. (c) Compensating line current and respective phase-to-neutral voltage.

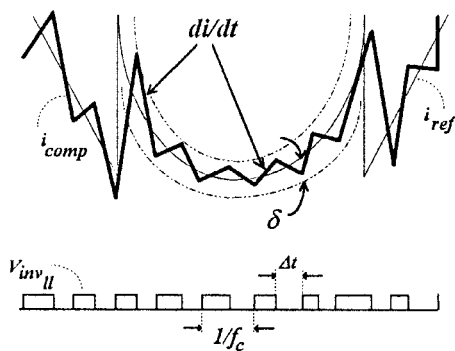


Fig. 8. The evolution of the inverter output current as a function of time.

current and voltage signals. The values of the link reactor and dc capacitor define the transient time response of each converter. The link reactor must allow the  $di/dt$  at the inverter output current required to follow the reference waveform imposed by the control system. The dc capacitor must be

able to keep the dc voltage constant under transient operating conditions resulting from fast changes in the load. Transient changes in the dc-bus voltage are also compensated for by the voltage control scheme.

1) *Link Reactor*: The maximum slope of the inverter output current may be obtained from (4). The evolution of the inverter output current is shown in Fig. 8. From this figure, the slope of the inverter generated current is equal to

$$\frac{\Delta i}{\Delta t} = \frac{2\delta}{\frac{1}{2f_c}} \quad (8)$$

By replacing (8) in (4), the value of  $L$  is obtained:

$$L = \frac{V_{inv} - E_0}{4 \cdot \delta \cdot f_c} \quad (9)$$

where  $V_{inv}$  is the inverter output voltage,  $E_0$  the instantaneous voltage of the ac source,  $\delta$  is the amplitude of the error current, and  $f_c$  is the maximum switching frequency.

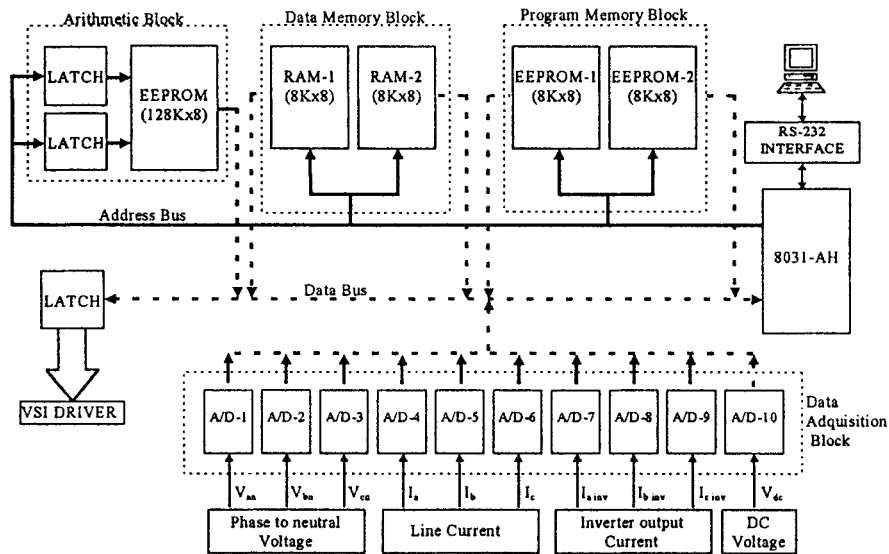


Fig. 9. The proposed control circuit topology for each converter.

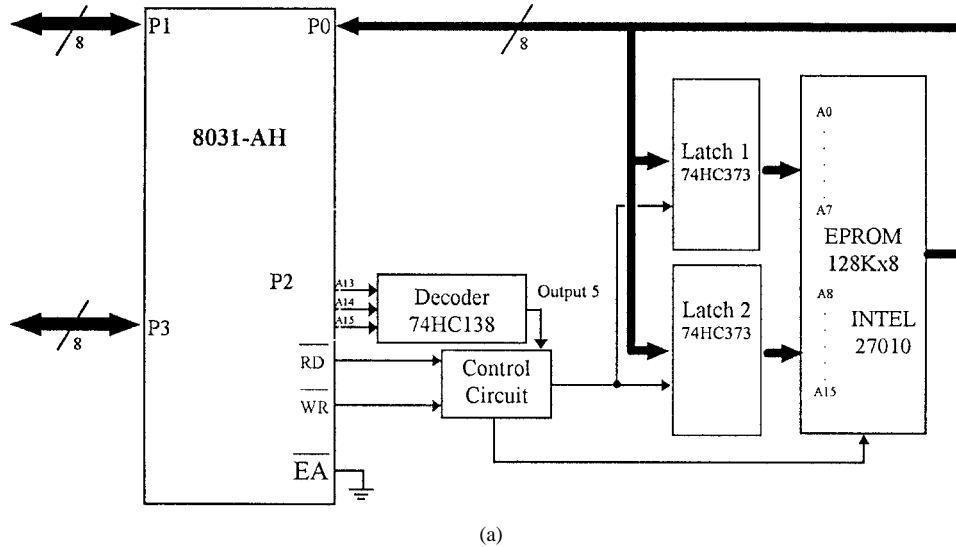


Fig. 10. (a) Block diagram of the hardware required for the multiplication of two 8-b numbers.

2) *DC Capacitor*: One of the selection criteria used to calculate the value of  $C$  is related to the maximum voltage fluctuation allowed in the dc bus when transient changes in the load occur. In this case, the value of  $C$  is obtained from the following equation:

$$C = \frac{1}{\Delta V} \int_{t_1}^{t_2} i_c(t) dt \quad (10)$$

where  $i_c(t)$  is the instantaneous current flowing through the dc capacitor and  $\Delta V$  is the voltage fluctuation of the dc bus.

3) *Inverters Rated Power*: High switching frequency in the converter increases commutation losses and imposes severe stresses in the semiconductor, specially when they commutate large rms current. For these reasons, the rated power of each converter is related to the switching frequency. In this case, the first inverter operates at 400 Hz (i.e., it can compensate for displacement power factor and the fifth and seventh current harmonic components), and the second operates at 1.5 kHz (it

compensates for only high-frequency current harmonics). For these switching frequencies, and considering a total harmonic distortion (THD) in the ac source current lower than 5%, the rated power of each converter with respect to the load rated power are 26% and 8.7%, respectively. Since the first converter also compensates for displacement power factor, its rated power converter may increase if the load power factor is smaller.

### B. Control Circuit Design

The proposed control circuit of each inverter is implemented with an INTEL 8031 AH microcontroller with 32 kbytes of memory composed by two blocks of 8 kbytes of electrically programmable read-only memory (EPROM) and two blocks of 8 kbytes of RAM (Fig. 9). The program stored in the EPROM's controls the PWM-VSI dc voltage, calculates the reference currents, and generates the gating signals of each inverter. The RAM is used to store the data required by

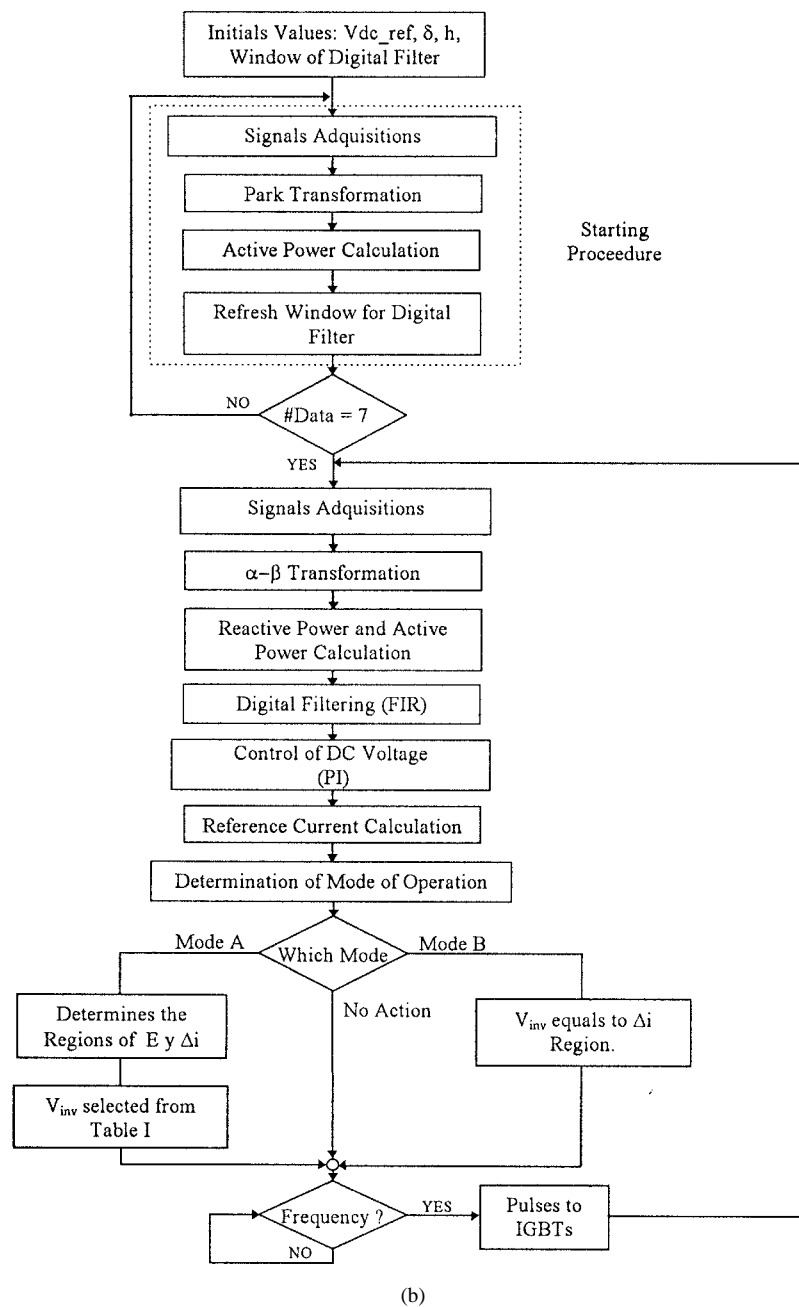


Fig. 10. (Continued) (b) Flowchart of the principal control program.

the main program (i.e., A/D conversion data, currents, and voltages in  $\alpha$ - $\beta$  reference frame, and reference currents). The microcontroller has an 8-b CPU that operates at 12 MHz. Ten ADC0820 converters are used to transform analog currents and voltages to digital signals. The time required by each A/D conversion is 1  $\mu$ s. It is important to note that the A/D conversion of the ten signals is done simultaneously (Fig. 9). The dc component of the active power is obtained through a low-pass finite impulse response (FIR) digital filter tuned at 90 Hz. For this type of application, this filter introduces a negligible phase shift between input and output signals. The set points of each PWM-VSI, i.e., switching frequency, ripple current factor, and dc voltage value can be changed by a host computer, through the communication between the com-

puter serial port with the internal 8-b universal asynchronous receiver transmitter (UART) of the microcontroller.

The mathematical expression of the FIR digital filter is the following [12]:

$$y(n) = \sum_{k=0}^M B_k x(n-k) = h(n) \cdot x(n); \quad k \geq \text{order} \quad (11)$$

where  $y(n)$  is the filter output signal and  $x(n)$  is the filter input signal. The filter constants  $h(n)$  were obtained using MATLAB software [13]. The constant values for each converter control scheme are shown in Table III, where VSI #1 represents the constant values used for the converter operating

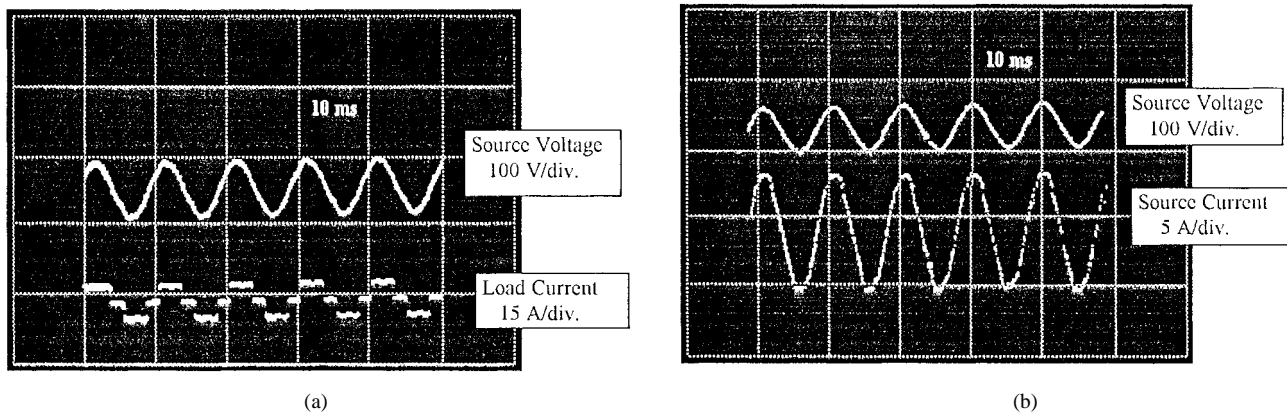


Fig. 11. Steady-state experimental results. (a) The phase-to-neutral source voltage (10 ms/div), 100 V/div, and the respective load current, 15 A/div. (b) The phase-to-neutral source voltage (20 ms/div), 100 V/div, and the respective source current, 5 A/div.

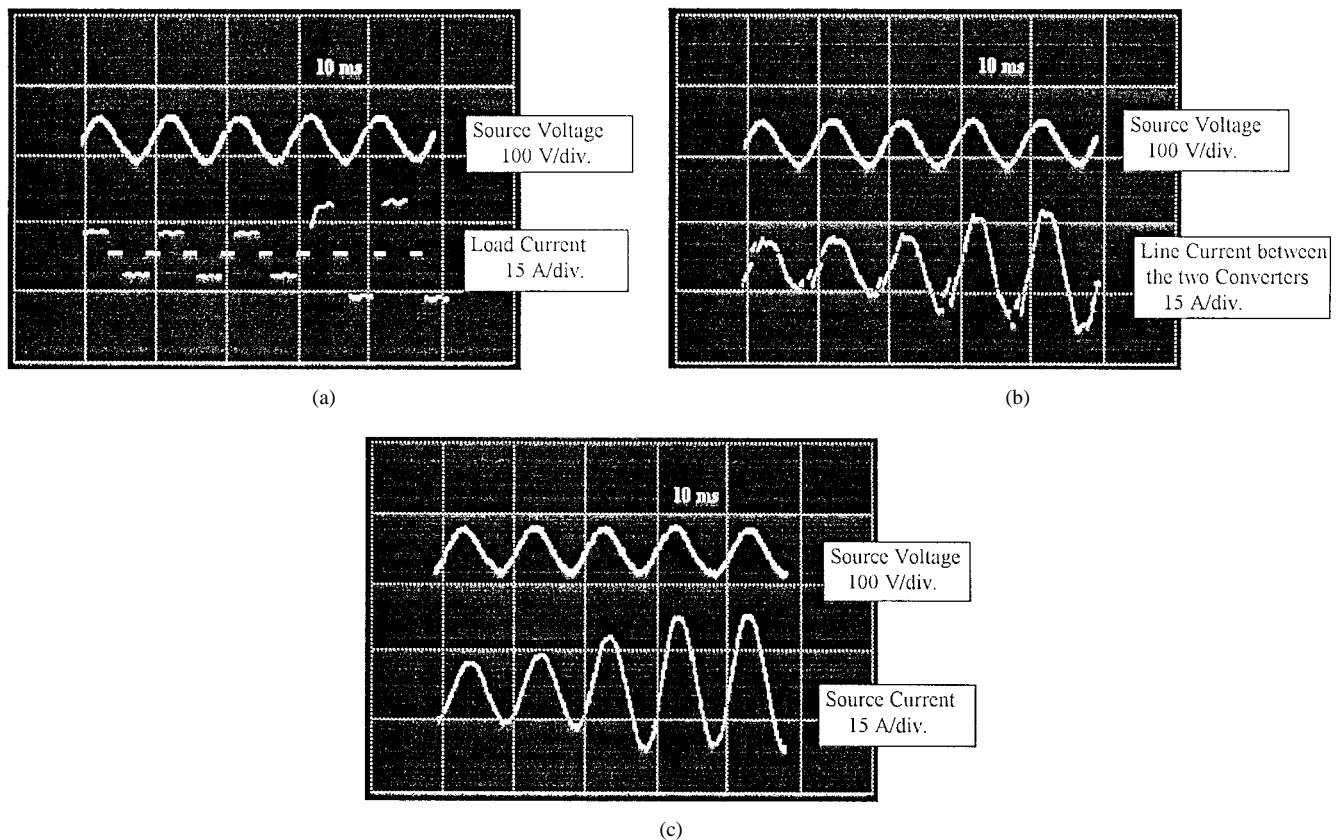


Fig. 12. Transient-state experimental results for a 20% step change in the load current (10 ms/div). (a) Source phase-to-neutral voltage, 100 V/div, and load current, 15 A/div. (b) Source phase-to-neutral voltage, 100 V/div, and the line current between the two inverters, 15 A/div. (c) Source phase-to-neutral voltage, 100 V/div, and the respective source current, 15 A/div.

at lower frequency (400 Hz) and VSI #2 for the inverter operating at 1.5 kHz. It is important to note that the FIR constants  $h(n)$  for each converter are different, since the sample frequency of the analog signals for the two control schemes are 400 Hz and 1.5 kHz, respectively. The execution time of the filter algorithm is 240  $\mu$ s.

In order to reduce the multiplication time between two 8-b numbers, a distributed arithmetic algorithm was implemented. With this algorithm, all the possible results between two bytes are stored in an external 128-kbyte EPROM, so that the

multiplication time is reduced to that necessary to address the memory location and to read from this memory location the result of the multiplication. It is important to note that the result is scaled to an 8-b representation. By using this method, the multiplication time between two 8-b variables is 2  $\mu$ s. The block diagram of the hardware implementation is shown in Fig. 10(a).

The total execution time of the active power filter control program is 650  $\mu$ s. The flowchart of the main program is shown in Fig. 10(b). At the beginning of the operation, the

TABLE III  
FIR CONSTANT VALUES  $h(n)$

Constant Value $h(n)$	VSI # 1	VSI # 2
h(1)	0.0080	0.0088
h(2)	0.0320	0.0479
h(3)	0.1585	0.1640
h(4)	0.3086	0.2793
h(5)	0.3096	0.2793
h(6)	0.1585	0.1640
h(7)	0.0320	0.0479
h(8)	0.0080	0.0088

digital FIR filter requires eight samples of the respective signal, and, for this reason, the main program does not start the operation until these samples are completed.

#### IV. EXPERIMENTAL RESULTS

A 10-kVA laboratory prototype using IGBT switches was implemented and successfully tested in compensating a six-pulses controlled rectifier. Inverter #1 is operating a 400-Hz switching frequency, connected to the ac line through a 180-mH link inductor, and a dc capacitor of 3.3 mF. Inverter #2 operates at 1.5-kHz switching frequency and is connected to the ac lines through a 90-mH link inductor and a dc capacitor of 2.2 mF. Relevant experimental results obtained with this breadboard unit are shown in Figs. 11 and 12.

#### V. CONCLUSIONS

In this paper, an active power filter implemented with two PWM-VSI's connected in cascade has been presented and analyzed. The control scheme of each PWM-VSI is implemented with an INTEL 8031 AH 8-b microcontroller. Each PWM-VSI operates at a different switching frequency, allowing the compensation of high-power nonlinear loads. The close agreement between the analytical and the experimental results proves the validity of the analysis and the feasibility of the proposed control scheme.

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