

Open-loop VAr compensator for industrial applications, using a single PWM pattern

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Abstract: The authors present the analysis of an open-loop, three-phase static VAr compensator (SVC) based on a voltage source inverter, using only one fixed pulse width modulation (PWM) pattern. The VAr generation is controlled by shifting this PWM pattern according to the AC-mains voltage. Because the system is naturally stable, there is no need to control the capacitor DC voltage, which takes a particular stable voltage for each power factor operation condition. To prove this particular behaviour, a stability analysis, based on the $d-q$ frame is developed. From this analysis, the circle diagram of the VAr compensator is obtained, which gives all the operating characteristics related to the DC voltage, power angle operation, and reactive power generated. The main characteristics of this compensator are its simplicity and its strong stability, which are particularly suitable for use in industrial loads, such as induction motors, thyristor rectifiers and other low power factor loads. This open-loop system is suitable in the range 1–20kvar. The experimental results confirm the operating characteristics given by computer simulations and analysis.

1 Introduction

The implementation of many kinds of converters, such as power rectifiers, power inverters and others, is possible thanks to the development of powerful semiconductor switches [1]. The same electronic components have also been used for reactive power compensation. In this field of application, the first step was taken using thyristor power converters and the line commutation principle [2, 3]. However, the inherent mode of operation of thyristor converters generates unwanted harmonics. This problem has been reduced by using force-commutated devices [4, 5].

The advantages of using force-commutated VAr compensators and special pulse width modulation (PWM) techniques have already been confirmed. Their practical implementation is today possible in the field

of medium and high levels of reactive power compensation thanks to the development of GTOs, high power IGBTs and other electronic devices. These PWM techniques permit a considerable reduction in harmonic distortion. Another advantage of force commutated VAr compensators, is that the generation of reactive power does not depend on the size of the capacitors used in the DC link [6].

However, force commutated PWM converters are much more complicated than thyristor VAr compensators, because they need special patterns of modulation, control blocks and feedback systems [7–9]. Searching for a simple design, this paper analyses the behaviour of a voltage source type, PWM VAr compensator, which works without any feedback voltage or current and also with only one, fixed PWM pattern. Some previous works have introduced the idea of using PWM with fixed switching frequency [10], but without a fixed PWM pattern. Additionally, there is no mention about operation under open-loop conditions. A previous paper [11] has shown the fixed PWM pattern concept, applied to a voltage source rectifier. Analytical demonstrations described in this paper, are confirmed by using digital computer simulations and experiments with a 2-kvar PWM compensator. These simulations also show that this kind of SVC could be suitable for industrial applications in the range 1–20kvar. This allows the compensation of loads such as induction motors or thyristor converters, in the range 1–100kVA.

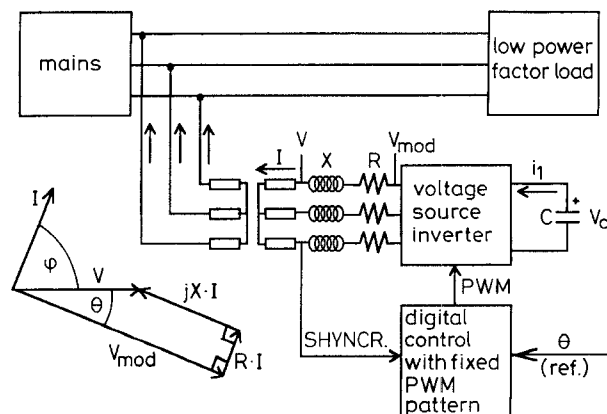


Fig. 1 Open-loop VAr compensator

2 Principle of operation

The heart of the proposed SVC is a conventional three-phase PWM voltage source inverter, as shown in Fig. 1. The SVC is directly connected in parallel, between the mains and the low power factor load. The

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DC link capacitor voltage is neither measured, nor controlled. The six switches of the SVC, which generate the modulated voltage v_{mod} , are controlled by a fixed PWM pattern, stored in an EPROM. The reactive power is controlled by changing the phase angle θ between the mains voltage V and V_{mod} . The V_{mod} is the fundamental component of the voltage v_{mod} , generated by the PWM pattern. Each time θ is modified, the capacitor voltage V_c changes to a new stable value. As V_c changes, the amplitude of the fundamental V_{mod} (generated by the fixed PWM pattern) also changes modifying the amount of reactive power generated. This reactive power basically depends on the difference of amplitude between the mains voltage V , and V_{mod} . It should be noted that the internal losses of the SVC play an essential role in keeping V_c stable.

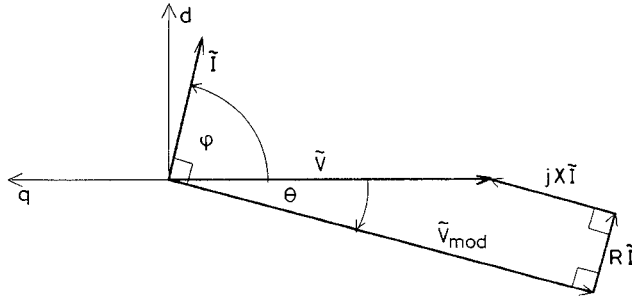


Fig. 2 Phasor diagram of the VAr compensator

3 Stability analysis

One simple way to analyse the stability of this open-loop SVC, is through the d-q frame. Fig. 2 shows the phasor diagram of the SVC in the d-q frame, where

- V = mains phase-to-neutral voltage
- V_{mod} = fundamental voltage generated by fixed PWM pattern
- $X = \omega L$ = input reactance of SVC
- R = input resistance, represents losses of SVC
- I = AC VAr compensator current
- d-q = reference frame

The losses of the SVC depend on the switching frequency (which is constant because the PWM pattern is fixed), on the DC voltage, and mainly on the AC currents. These losses can be approximately represented by the input resistance R (shown in Fig. 1), through the term $3RI^2$. As the PWM pattern is fixed, the relation between the DC voltage v_c , and the instantaneous value of the amplitude of V_{mod} is constant

$$|V_{mod}| = K_V \cdot v_c \quad (1)$$

The dynamic equation of the modulator can be written in d-q axis as

$$\begin{bmatrix} L & 0 \\ 0 & L \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} R & -X \\ X & R \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} v_d \\ v_q \end{bmatrix} - \begin{bmatrix} v_{mod_d} \\ v_{mod_q} \end{bmatrix} \quad (2)$$

where

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} 0 \\ -V\sqrt{3} \end{bmatrix} \quad (3)$$

Eqn. 3 represents the mains voltage in the d-q frame. By introducing eqn. 3 into eqn. 2, and because $X = \omega L$, it yields

$$\frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = -\frac{1}{L} \begin{bmatrix} v_{mod_d} \\ v_{mod_q} + V\sqrt{3} \end{bmatrix} - \begin{bmatrix} \frac{R}{L} & -\omega \\ \omega & \frac{R}{L} \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad (4)$$

v_{mod_d} and v_{mod_q} are related through the reference angle θ

$$\frac{v_{mod_q}}{v_{mod_d}} = -\text{ctg} \theta = \sigma_V \quad (5)$$

The instantaneous value of the amplitude of V_{mod} , in terms of its d-q components, is expressed as

$$|V_{mod}| = \frac{1}{\sqrt{3}} \sqrt{v_{mod_d}^2 + v_{mod_q}^2} \quad (6)$$

Combining eqns. 1, 5 and 6 allows one to obtain relationships between v_{mod_d} and v_{mod_q} with the DC voltage v_c

$$v_{mod_d} = \frac{\sqrt{3}k_v}{\sqrt{1 + \sigma_v^2}} \cdot v_c = K_d \cdot v_c \quad (7)$$

$$v_{mod_q} = K_d \cdot \sigma_v \cdot v_c = K_q \cdot v_c \quad (8)$$

Substituting eqns. 7 and 8 into eqn. 4, yields

$$\frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = -\frac{1}{L} \begin{bmatrix} K_d \cdot v_c \\ K_q \cdot v_c + \sqrt{3} \cdot V \end{bmatrix} - \begin{bmatrix} \frac{R}{L} & -\omega \\ \omega & \frac{R}{L} \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad (9)$$

There are two equations in eqn. 9 and three unknown values: v_c , i_d and i_q . A third equation is therefore required. The power balance equation and the DC capacitor voltage equation solve the problem

$$v_c \cdot i_1 = v_{mod_d} \cdot i_d + v_{mod_q} \cdot i_q \quad (10)$$

$$i_1 = C \cdot \frac{dv_c}{dt} \quad (11)$$

By substituting eqns. 7, 8 and 11 into eqn. 10 we obtain

$$C \cdot \frac{dv_c}{dt} = K_d \cdot i_d + K_q \cdot i_q \quad (12)$$

Eqn. 12 is the third equation required to solve the problem. Now there are three equations for three unknown values: v_c , i_d and i_q

$$\frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ v_c \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega & -\frac{K_d}{L} \\ -\omega & -\frac{R}{L} & -\frac{K_q}{L} \\ \frac{K_d}{C} & \frac{K_q}{C} & 0 \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \\ v_c \end{bmatrix} - \frac{1}{L} \begin{bmatrix} 0 \\ V\sqrt{3} \\ 0 \end{bmatrix} \quad (13)$$

or

$$\dot{\mathbf{x}} = [A] \cdot \mathbf{x} + \mathbf{B} \quad (14)$$

where

$$[A] = \begin{bmatrix} -\frac{R}{L} & \omega & -\frac{K_d}{L} \\ -\omega & -\frac{R}{L} & -\frac{K_q}{L} \\ \frac{K_d}{C} & \frac{K_q}{C} & 0 \end{bmatrix} \quad (15)$$

The stability of the system can be found through the eigenvalues of the $[A]$ -matrix

$$\det\{S[I] - [A]\} = 0 \quad (16)$$

or

$$a_0 \cdot s^3 + a_1 \cdot s^2 + a_2 \cdot s + a_3 = 0 \quad (17)$$

where

$$\begin{aligned} a_0 &= 1, \\ a_1 &= 2R/L \\ a_2 &= (K_d^2 + K_q^2)/LC + (R/L)^2 + \omega^2 \\ a_3 &= R(K_d^2 + K_q^2)/L^2C \end{aligned}$$

Applying Routh's criterion for stability, ($a_i > 0 \forall i$ and $a_1 a_2 - a_0 a_3 > 0$), one finds that the system is always stable, because in real systems $R > 0$, $L > 0$, and $C > 0$. The consequence of this result is that, with respect to

R , this open-loop SVC is always stable, because it is not possible to have a practical device with theoretically zero losses ($R = 0$). On the other hand, the inductance L is always needed in this kind of converter. Another important consequence of this analysis is that the stability does not depend on the size of the DC capacitor. The capacitor has to be dimensioned based on other design restrictions such as transient response or ripple in the DC link.

4 Steady-state operation

Under steady-state operation $\dot{x} = 0$ and then

$$K_d \cdot V_C + R \cdot I_d - X \cdot I_q = 0 \quad (18)$$

$$K_q \cdot V_C + X \cdot I_d + R \cdot I_q = -V\sqrt{3} \quad (19)$$

$$K_d \cdot I_d + K_q \cdot I_q = 0 \quad (20)$$

From eqns. 18–20 one obtains an expression for V_C under steady-state conditions

$$V_C = -V\sqrt{3} \cdot \frac{R \cdot K_q + X \cdot K_d}{R(K_d^2 + K_q^2)} \quad (21)$$

but because of eqns. 7, 8 and 5

$$V_C = V \frac{R \cdot \text{ctg} \theta - X}{R \cdot K_V} \sin \theta \quad (22)$$

$$V_C = \frac{V(R \cos \theta - X \sin \theta)}{R \cdot K_V} \quad (23)$$

K_V is a constant which depends on the switching pattern of the compensator. By substituting eqn. 1 into eqn. 23 it yields

$$|V_{mod}| = V \left(\cos \theta - \frac{X}{R} \sin \theta \right) \quad (24)$$

4.1 The circle diagram

Eqn. 24 represents the equation of a circle in polar coordinates. This circle diagram shown in Fig. 3, relates the magnitude of V_{mod} (and hence the magnitude of V_C) for different values of the reference θ . The direction of I is the same as $R \cdot I$ in the diagram.

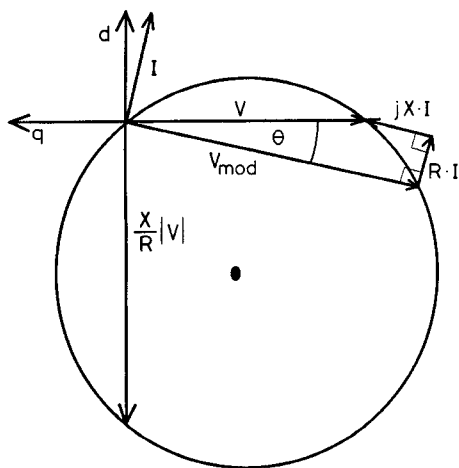


Fig. 3 Circle diagram of the VAR compensator

It can be observed from the circle diagram of the SVC that the larger the X/R ratio, the longer is the diameter of the circle. With large X/R ratios, the system becomes very sensitive, because small changes in the θ reference produce large variations in $|V_{mod}|$ and consequently in V_C . Since this situation is specially true in large SVCs, open loop operation is not recommendable

for those cases. Computer simulations show that a suitable range of utilisation for open-loop SVCs is 1–20kvar.

The circle diagram of Fig. 3 also shows that when θ is positive, V_{mod} leads the mains V , and the magnitude of V_{mod} becomes smaller than the magnitude of V . In such a case, the SVC absorbs reactive power. On the other hand, when θ is negative, V_{mod} lags the voltage V . In this case, the system generates reactive power, because $|V_{mod}|$ becomes larger than $|V|$.

The circle diagram also permits us to realise what would happen if R were neglected in the analysis. In such a situation, the circle diagram would have an infinite radius, and therefore no possible equilibrium point for V_{mod} could be found. As a consequence, the open-loop SVC would not be able to work.

4.2 Reactive power generation and power losses

The generation of reactive power depends on the I_d magnitude. When $I_d > 0$ the SVC generates reactive power. From eqns. 18–20

$$I_d = \frac{V \cdot \sqrt{3}}{R \left(\frac{K_q}{K_d} + \frac{K_d}{K_q} \right)} \quad (25)$$

But because of eqns. 5, 7 and 8

$$\frac{K_q}{K_d} = -\text{ctg} \theta \quad (26)$$

$$I_d = -\frac{V\sqrt{3}}{2R} \sin 2\theta \quad (27)$$

In the d-q frame the reactive power is

$$Q = -V_q \cdot I_d = V\sqrt{3} \cdot I_d \quad (28)$$

and finally, from eqns. 27 and 28

$$Q = -\frac{3V^2}{2R} \sin 2\theta \quad (29)$$

Plotting the magnitude of Q as a function of the reference angle θ , one obtains the graphic shown in Fig. 4.

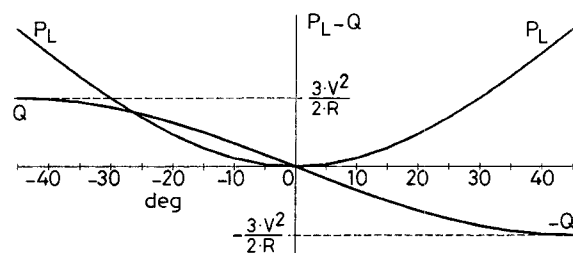


Fig. 4 Reactive power and power losses against θ angle characteristic

It can be observed from Fig. 4 that the maximum reactive power that can be produced is equal to

$$Q_{max} = \frac{3}{2} \cdot \frac{V^2}{R} \quad (30)$$

and it occurs when $\theta = 45^\circ$. However, the operation limits of the SVC should be restricted to small angles ($\theta < 10^\circ$). Otherwise, the power losses become too large. The power losses of the converter are unavoidable but at the same time necessary for the stability in open-loop operation. The power losses can also be evaluated in the d-q frame, and they depend on the magnitude of I_q

$$P_L = V_q \cdot I_q = -V\sqrt{3} \cdot I_q \quad (31)$$

I_q can be obtained from eqns. 18–20, and with the help of eqns. 5, 7 and 8

$$I_q = -\frac{V\sqrt{3}}{R} \sin^2 \theta \quad (32)$$

combining eqn. 31 with eqn. 32

$$P_L = \frac{3V^2}{R} \sin^2 \theta \quad (33)$$

Because of the quadratic characteristic of eqn. 33, the power losses are always positive (they have a maximum value at $\theta = \pm 90^\circ$). For comparison purposes, Fig. 4 shows simultaneously, the reactive power and the power losses against θ angle characteristic.

Due to the term $\sin^2 \theta$, the power losses become important when θ is large. For small angles, the Q/P_L relation is more advantageous and practical. From eqns. 29 and 33

$$\left| \frac{Q}{P_L} \right| = \frac{\sin 2\theta}{2 \sin^2 \theta} = |\operatorname{ctg} \theta| = |\sigma_V| \quad (34)$$

Plotting eqn. 34 one obtains the graphic shown in Fig. 5, which is independent of the SVC parameters. Fig. 5 clearly shows that the angle of operation of the SVC should be restricted to small angles. Otherwise the losses related to reactive power generation become too large. A close-up of Fig. 4 is shown in Fig. 6, where θ is in the range $\pm 5^\circ$. In this range, the SVC will operate with high efficiency.

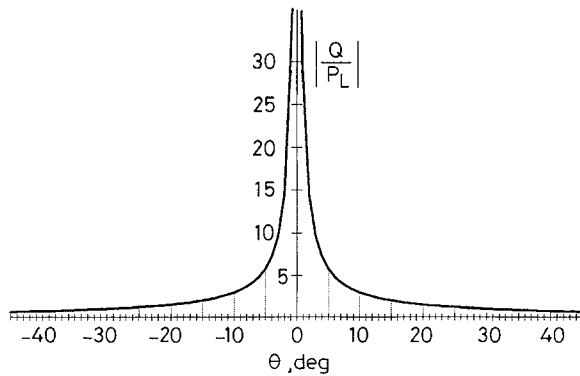


Fig. 5 $|Q/P_L|$ against θ angle

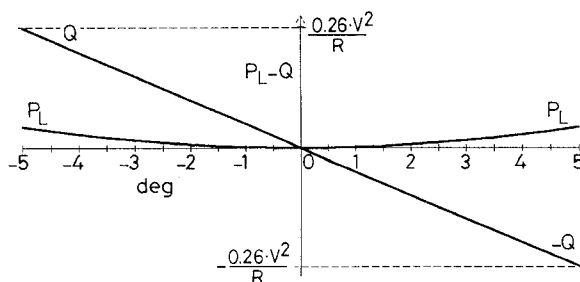


Fig. 6 Reactive power and power losses in the interval $\theta = (-5^\circ, 5^\circ)$

4.3 Power losses in the DC link

Until now, the power losses of the DC capacitor have been neglected. However, it is important to emphasise that they do not affect the stability of the open-loop SVC. They can be incorporated into the analysis by adding a resistor in parallel with the DC capacitor. In such a case, the capacitor equation (eqn. 11) becomes

$$C \frac{dv_C}{dt} = i_1 - \frac{v_C}{R_C} \quad (35)$$

Repeating all the previous procedures, the matrix $[A]$

(eqn. 15) becomes

$$[A] = \begin{bmatrix} -\frac{R}{L} & \omega & -\frac{K_d}{L} \\ -\omega & -\frac{R}{L} & -\frac{K_q}{L} \\ \frac{K_d}{L} & \frac{K_q}{L} & -\frac{1}{RC} \end{bmatrix} \quad (36)$$

Similar analysis of stability permits one to realise that the system is also stable when $R > 0$. Then, these losses do not affect the stability under open-loop conditions.

5 Simulations and experimental results

The performance characteristics of the open-loop SVC have been verified by digital computer simulations. The 'valve-by-valve' digital simulation developed for the compensator, is based on treating the three-phase bridge as a piecewise circuit problem. The on-off states of each of the six power switches give rise to eight possible circuit topologies. The instants of switching of the semiconductors are defined by the switching pattern adopted, which is only one. The switching pattern is synchronised with the mains, generating a fundamental V_{mod} which is shifted with respect to the mains at the desired reference θ . The differential equations, arising from the Kirchhoff voltage and current laws for the topologies, are solved by the requirements that the flux linkages and electric charges must be continuous. Changing the θ angle, different operating conditions can be obtained. Pascal and Quick-Basic were used for simulations. The advantages of working with simulations are that they allow one to visualise the behaviour of very large VAR compensators and also they permit good tuning of the design.

For experimental results, a 2-kvar compensator has been implemented. It was built using 600V, 30A, modular Darlington bipolar transistors and simplified driver circuits with hybrid components. The control block was implemented with a simple EPROM, with only one pattern stored, synchronised with the frequency mains. The θ angle reference is controlled by a digital adder and is modified manually. Input inductances have been constructed using toroidal-core ferrites with a small air gap to avoid saturation. The DC link has a 1500 μ F electrolytic capacitor. This value has been adopted only for DC ripple considerations.

The start-up of the system is simple: when connected, the power transistors remain inhibited, and the DC capacitor is charged through the antiparallel diodes of the transistors, and through a limiting resistor. When the DC capacitor is fully charged, the limiting resistor is short-circuited, and the control system, which is already producing the synchronised switching pattern, is automatically connected to the transistor drivers. At this moment the compensator begins to operate.

5.1 Lagging power factor

Lagging power factor operation of the open-loop SVC has been tested, using simulations and experiments. The oscillograms of Figs. 7 and 8, respectively, show a computer simulation, and an experimental result for this mode of operation. The parameters for both, the simulation and the experiment, are the same: $V = 90$ V (max), $V_c = 250$ V, $R = 1.5 \Omega$, $L = 5$ mH, and $C = 1500 \mu$ F. The RMS current is 6A. The switching pattern in both cases is also the same: an overmodulated sinusoidal PWM with a triangular carrier. It can be observed that the two cases (simulation and experiment) have very similar waveforms. These results show

that the simulation package developed (which was also used to obtain a 'simulated' circle diagram), is a good tool for the design of the open-loop SVC.

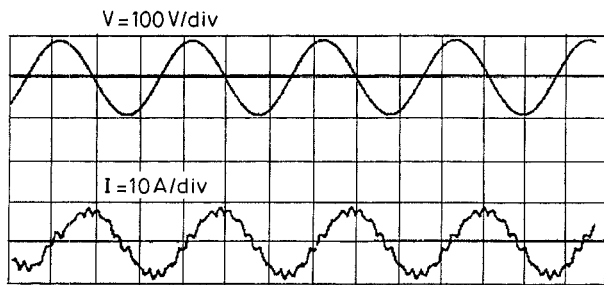


Fig. 7 Lagging oscillograms for $V = 90\text{ V (max)}$, $V_c = 250\text{ V}$, and $f = 50\text{ Hz}$
Simulation

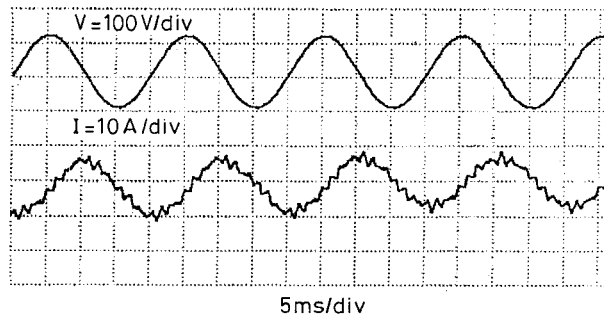


Fig. 8 Lagging oscillograms for $V = 90\text{ V (max)}$, $V_c = 250\text{ V}$, and $f = 50\text{ Hz}$
Experimental results

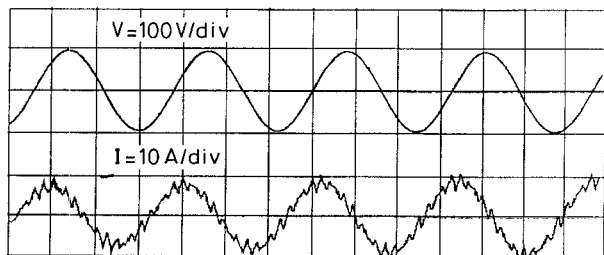


Fig. 9 Leading oscillograms for $V = 90\text{ V (max)}$, $V_c = 300\text{ V}$, and $f = 50\text{ Hz}$
Simulation

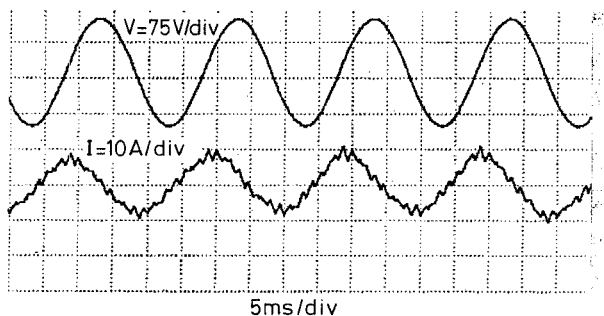


Fig. 10 Leading oscillograms for $V = 90\text{ V (max)}$, $V_c = 300\text{ V}$, and $f = 50\text{ Hz}$
Experimental results

5.2 Leading power factor

The oscillograms of Figs. 9 and 10, respectively, show a computer simulation and an experimental result for a leading power factor operation. The parameters are the same as for the lagging operation, and the RMS current is 6.5A. The switching pattern is the same in both cases, and also the same as the one used in the previous lagging power factor oscillograms (see Figs. 7 and 8).

During leading power factor operation, the SVC works with a modulated voltage V_{mod} larger than the mains voltage, V . The DC voltage V_c depends directly on V_{mod} and hence it is also larger than the value it takes under lagging power factor operation, reaching here 300V DC. The larger the Q generated, the larger the DC voltage. As a consequence, the generation of large amounts of reactive power could produce voltage stresses in the power switches, and also in the DC capacitor. For this reason, the reactive power generation depends on both the current and voltage ratings of the electronic switches, and also on the voltage rating of the DC capacitor.

5.3 Transient response

The computer simulations demonstrate that the dynamic behaviour of the open-loop VAr compensator mainly depends on the size of the DC capacitor. The smaller the DC capacitor, the faster the transient response. The simulation of Fig. 11 shows the behaviour of the SVC, with 1500 μ F, and Fig. 12 shows it with 500 μ F, DC capacitor. The transient response is faster in Fig. 12, but the DC voltage ripple becomes visible. However, it is a matter of improving the switching pattern to keep the ripple low with small DC capacitors. Faster response and low ripple content have to be properly balanced.

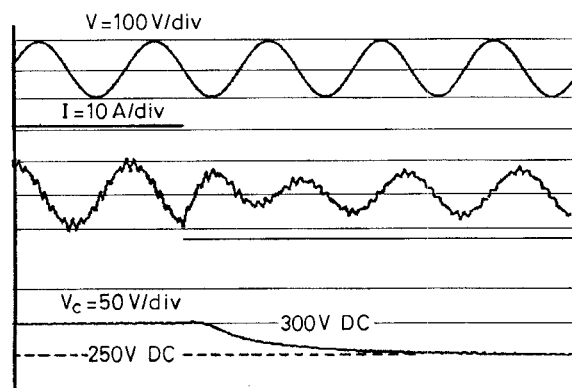


Fig. 11 Step reversal simulation from leading to lagging current
 $C = 1500\ \mu\text{F}$

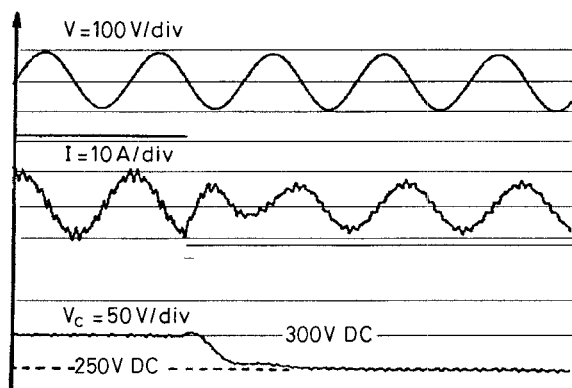


Fig. 12 Step reversal simulation from leading to lagging current
 $C = 500\ \mu\text{F}$

Fig. 13 shows an experimental result using a 1500 μ F electrolytic capacitor. In this experiment, the AC current of the laboratory prototype changes from 8A leading to 6A lagging. As can be seen, the response is not as good as in the simulations. This is mainly because of

a poor regulation of the mains used in the laboratory. Another problem is the synchronisation signal which has to be improved.

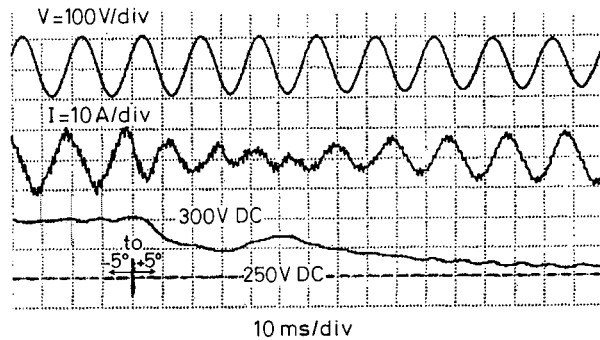


Fig. 13 Step reversal experiment from leading to lagging current

6 Conclusions

A simple, open-loop control, PWM static VAR compensator (SVC) for industrial applications has been proposed and analysed. It uses only one fixed PWM pattern stored in an EPROM, and the VAR generation is controlled by shifting this pattern with respect to the mains voltage. The system in itself is naturally stable, which means that no control is needed on the DC capacitor voltage. A complete stability analysis, based on the d-q frame, has been developed. From this analysis, the circle diagram of the open-loop SVC was obtained, which gave all the operating characteristics related to the DC voltage, power angle operation, and the amount of reactive power generated. This open-loop SVC shows special applications in industrial loads, such as induction motors, thyristor rectifiers and other low power factor loads, being useful in the range 1–20kvar. The main characteristics of this compensator are its simplicity and its strong stability, which does not depend on the size of the DC capacitor. On the other hand, from computer simulations it was possible to

realise that the dynamic response does depend on the size of the DC capacitor. Simulations and experiments confirm the results obtained in the theoretical analysis.

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