

A NEW CURRENT CONTROL STRATEGY FOR ACTIVE POWER FILTERS USING THREE PWM VOLTAGE SOURCE INVERTERS

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ABSTRACT: A new current control strategy for active power filters using multiple PWM voltage-source inverters is presented and analyzed in this paper. This technique allows to compensate high power non linear loads. The proposed current control strategy operates each PWM voltage-source inverter with a different switching frequency generating specific current harmonic components of the load. Reactive power is compensated without sensing and computing the reactive component of the load current, thus simplifying the control circuit. Current harmonics compensation is done in time domain. The active power filter presented in this paper is implemented with three PWM voltage-source inverters connected to a self controlled dc bus. In particular, this paper discusses the proposed scheme in terms of principles of operation, power and control system design, and the analysis under steady-state and transient operating conditions. Simulated results obtained for steady-state and transient operating conditions are presented and validated on a 20 kVA experimental unit.

INTRODUCTION

With the proliferation of active and non linear loads, including the increasing number of static power converters and arc furnaces, fast acting power filters will have to be considered as an essential component of a power distribution installation. In recent years, active power filters have been researched and developed to suppress harmonics generated by static power converters and large capacity power apparatus [1]. Various power circuit configurations have been proposed, and gradually being recognized as a viable solution to the problems created by harmonic components [2] - [8].

The topology of the three-phase active power filter presented in this paper is shown in Fig. 1. It can compensate for displacement and distortion power factor value. The proposed configuration is based on three force-commutated pulse-width modulated voltage-source

inverters connected in parallel to a self controlled dc bus. The ac terminals of each converter are connected to the power source through the filter reactors, X_1 . The control system of the active power filter consists of three modules, the low pass filter circuits for the generation of the compensating current reference signals required for each PWM converter, the current control circuits of the PWM inverters, and the control circuit for the dc capacitor voltage. Although there are a number of articles which deal with the analysis of active power filters using PWM voltage-source inverters, [2] - [8], the three-phase active power filter presented in this paper differs from previously discussed approaches in the following ways:

- a) Each PWM voltage-source inverter operates with different switching frequency allowing the generation of specific current harmonic component of the non linear load. In this way, the PWM inverter operating at the lowest switching frequency is in charge of the compensation of low frequency load current harmonics, while the second PWM inverter operates at medium switching frequency and compensates the medium frequency load current harmonics, and the third PWM inverter operates at high switching frequency generating the high frequency current harmonic components required by the load.
- b) Since low frequency current harmonics present the largest magnitude in power distribution systems, the voltage-source inverter operating at the lowest switching frequency is designed with the highest rated power. The PWM voltage-source inverters operating at medium and high switching frequency are rated for smaller values of rms current. In that way the PWM inverter operating with low switching frequency can be implemented using GTO switching devices or fast thyristors, which can stand larger rated current, while the other PWM inverters can use faster switches since they operate with smaller rated current.

- c) Current control in each PWM inverter is achieved with fixed switching frequency.
- d) It can compensate harmonic current component and reactive power simultaneously.
- e) Current control is done in time domain allowing instantaneous compensation.

Moreover, compared with active power filters using quad series PWM inverters [7], the proposed topology requires only three PWM voltage-source inverters, each inverter operating with a different and well defined switching frequency.

The treatment presented in this paper includes a comprehensive steady state and transient analysis of the proposed system, and the design of the power and control circuits. Special emphasis is given to the transient behavior of the active filter while it is compensating a non linear load. Finally, the validity of the active power filter is confirmed experimentally.

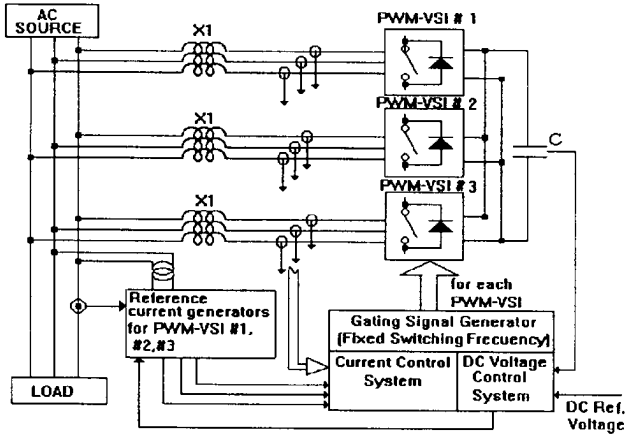


Fig. 1. The active power filter configuration.

II.- PRINCIPLES OF OPERATION

It is well known that active power filters correct current system distortion caused by non linear loads by injecting equal-but-opposite current harmonic components at specific points of a power distribution system [2]. The active power filter behavior under steady-state and transient operating conditions depends mainly on the control strategy. The control system has to be able to generate the current reference waveform for each PWM converter, maintain the dc bus voltage constant, and also has to produce the inverter gating signals. The block diagram of the active power filter control system presented in this paper is shown in Fig. 2. A brief functional description of each of the control system units proposed in this paper is given in the next three subsections.

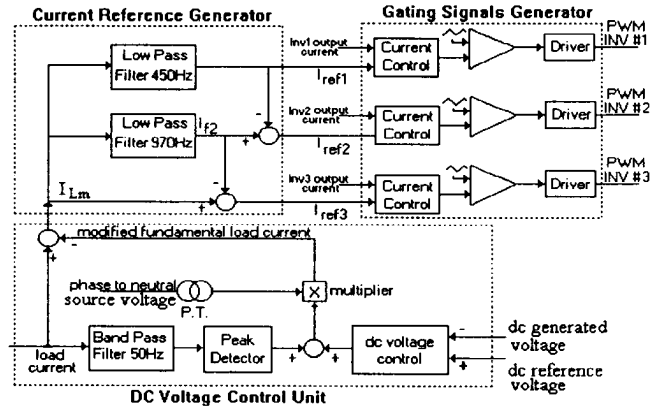


Fig. 2. The block diagram of the active power filter control system.

A) Current Reference Generator

The current reference generator circuit defines the compensation characteristics and accuracy of the active power filter. The current reference generator is composed mainly by two low-pass passive filters. Specifically, the inverter operating at low frequency (450 Hz) uses a second order filter with a corner frequency equals to 450 Hz. It is important to notice that the input current of the low pass filters is equal to the load current (included all the harmonic components) minus a modified fundamental current component. The modified fundamental current component is in phase with the respective phase to neutral voltage, and is equal to the amplitude of the fundamental component of the load current plus or minus a signal generated by the dc voltage control unit (in order to keep the dc voltage constant). The current reference waveform required by the inverter operating at 970 Hz is obtained from a second order low pass filter with a corner frequency equals to 970 Hz minus the reference current waveform of the first PWM inverter, I_{ref1} . Finally, the current reference waveform required by the third PWM inverter, which operates at 1.6 KHz, is equal to the current I_{Lm} (Fig. 2), minus the output current reference waveform of the second order filter tuned at 970 Hz, I_{f2} (Fig. 2). The current, I_{Lm} , is equal to the total load current minus the modified fundamental load current.

The phase shift errors introduced by the second order low pass filters are automatically compensated by the current reference of the second and the third PWM inverters (I_{ref2} , I_{ref3}). The cancellation of the phase shift error presents in I_{ref1} is done by making the difference between the reference current of the first PWM inverter (I_{ref1}) and the output waveform of the low pass filter tuned at 970 Hz (I_{f2}), which generates I_{ref2} , and by making the difference between I_{Lm} and I_{f2} , so that the phase shift error in I_{ref1} is compensated by I_{ref2} and I_{ref3} , and the phase shift error

of I_{ref2} is compensated by I_{ref3} . Figures 3, 4, 5, and 6 show the current reference waveforms of each PWM voltage source inverter while compensating a six-step rectifier.

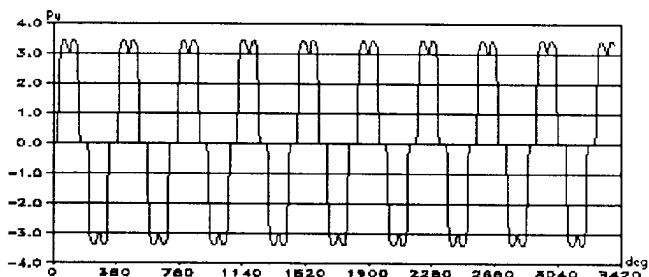


Fig. 3. Non linear load current.

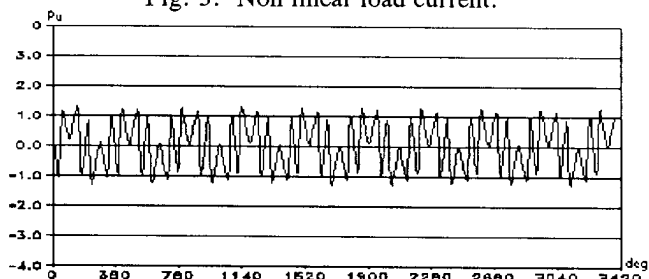


Fig. 4. The current reference waveform I_{ref1} .

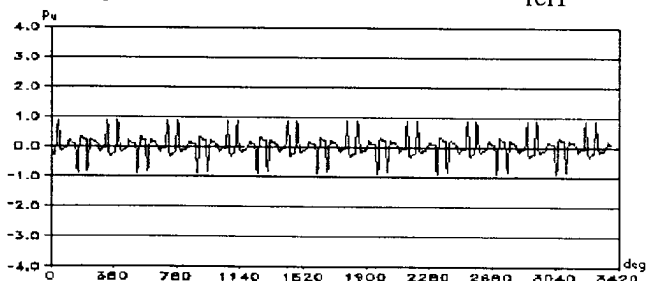


Fig. 5. The current reference waveform I_{ref2} .

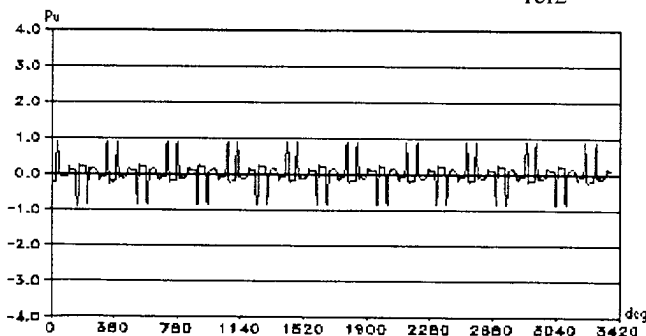


Fig. 6. The current reference waveform I_{ref3} .

Figures 5 and 6 show that I_{ref2} and I_{ref3} are very similar. However, in Fig. 7 the same waveforms are

superimposed and the difference in the phase-shift becomes clear.

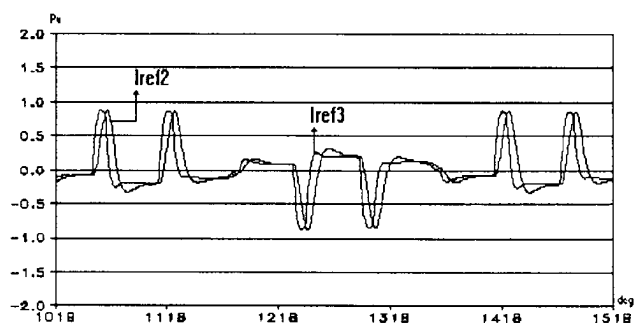


Fig. 7. The current reference waveforms I_{ref2} and I_{ref3} .

B) DC Voltage Control Unit

Voltage control in the dc bus is performed by adjusting the small amount of real power flowing into the dc capacitor. The real power flowing into the active power filter depends on the amplitude and phase-shift of the fundamental component of the current reference waveform of the low frequency PWM inverter, I_{Lm} (Fig. 2). The inverters operating at medium and high switching frequency generate only harmonic current components and do not have any influence in the dc capacitor voltage value.

By controlling the amplitude of I_{Lm} , the low frequency PWM inverter absorbs the real power required to cover the inverters switching losses and to maintain the steady state dc capacitor voltage constant. Also, since I_{Lm} leads the respective ac source phase to neutral voltage, the low frequency PWM inverter generates or absorbs the reactive power required to compensate the load displacement power factor.

C) Gating Signals Generator

The gating signals applied to each PWM voltage source inverter are defined by comparing the current error signal obtained from the Current Reference Generator Circuit with a fixed frequency triangular waveform (Fig. 2). The purpose of introducing the triangular waveform is to stabilize the inverter switching frequency, forcing it to be constant and equal to the frequency of the triangular waveform. The inverter is switched each time the two curves cross. In this current control technique, the current error is forced to remain within a window defined by the amplitude of the triangular waveform. This method can be explained by considering the bang-bang hysteresis technique plus the addition of a fixed frequency triangular waveform inside the imaginary hysteresis window [9].

III.- POWER CIRCUIT DESIGN

The values of the synchronous link reactor, X_L , and the dc capacitor, C , define the transient behavior of the active power filter. The value of the dc capacitor not only defines the amplitude of the high frequency ripple voltage across the dc bus, but also controls transiently the voltage fluctuations during fast changes in the load instantaneous power. In order to keep the inverters switching frequency constant, the slope of the current error signal must be slower than the slope of the triangular waveform (Fig. 2). The slope of the current error signal depends on the maximum slope of the inverter ac line current which is in turn fixed by the maximum instantaneous voltage drop across the inductor and the value of the inductance.

A) Design of the Synchronous Link Reactor

The design of the synchronous link reactor is performed with the constraint that for a given switching frequency the minimum slope of the inductor current is smaller than the slope of the triangular waveform that defines the switching frequency. In this way, the current error signal is forced to remain between the maximum and the minimum of the triangular waveform and as a result the inverter line current follows the reference signal closely.

The slope of the triangular waveform is defined by:

$$\lambda = 4\xi f_t \quad (1)$$

where ξ is the amplitude of the triangular waveform, which has to be equal to the maximum amplitude permitted in the high frequency ripple current, and f_t is the frequency of the inverter switching frequency (i.e., the frequency of the triangular waveform). The maximum slope of the inverter line current is equal to:

$$\frac{di}{dt} = \frac{V_{an} + 0.5V_{dc}}{L} \quad (2)$$

In order to ensure that the intersection between the current error signal and the triangular waveform exists, the slope of the inductor current has to be smaller than the slope of the triangular waveform, from (1) and (2):

$$L = \frac{V_{an} + 0.5V_{dc}}{4\xi f_t} \quad (3)$$

B) Design of the Dc Capacitor

Transient changes in the instantaneous power absorbed by the load generate voltage fluctuations in the dc voltage.

The amplitude of these voltage fluctuation can be controlled effectively with an appropriate dc capacitor value. It must be notice that the dc voltage control loop stabilizes the capacitor voltage after few cycles, but is not fast enough to limit the first voltage variations. The capacitor value obtained with this criteria is bigger than the value obtained based on maximum dc voltage ripple constraint. For this reason, the voltage across the dc capacitor presents a smaller harmonic distortion factor.

The maximum overvoltage generated across the dc capacitor is given by:

$$V_{cmax} = \frac{1}{C} \int_{t_1}^{t_2} i_c(t) dt + V_{dc} \quad (4)$$

where V_{cmax} is the maximum voltage across the dc capacitor,
 V_{dc} is the steady state average dc voltage,
 $i_c(t)$ is the instantaneous dc bus current.

From (4):

$$C = \frac{1}{\Delta V} \int_{t_1}^{t_2} i_c(t) dt \quad (5)$$

Equation (5) defines the value of the dc capacitor that will keep the transient voltage fluctuations across the dc bus below ΔV p.u.. The instantaneous value of the dc current is defined by the product of the inverter line currents with the respective switching functions. The average value of the dc current that generates the maximum overvoltage can be estimated by:

$$\int_{t_1}^{t_2} i_c(t) dt = I_{inv} \int_{t_1}^{t_2} [\{\sin(\omega t) + \sin(\omega t + 120^\circ)\} dt] \quad (6)$$

In this expression the inverter line current is assumed to be sinusoidal. This operating conditions represents the worst case.

IV.- CONTROL CIRCUIT DESIGN

The design procedure for the current and voltage loops is based on the respective time response requirements. Since the transient response of the active power filter is determined by the current control loop, its time response has to be fast enough to follow the current reference waveform closely. On the other hand, the time response of the dc voltage control loop need not to be fast and is

selected to be at least 10 times slower than the current loop time response of the inverter operating at 450 Hz. Thus, these two control systems can be decoupled and designed as two independent systems.

A PI controller are selected for the current and the voltage control loops since it contributes to zero steady state error in tracking the reference current and voltage signals respectively.

A) Design of the Current Control Loop

Each PWM inverter current control loop consists of three independent PI controllers. Since the active power filter is implemented with voltage-source inverters, the ac output current is defined by the inverter ac output voltage. The block diagram of the current control loop for each phase is shown in Fig. 8.

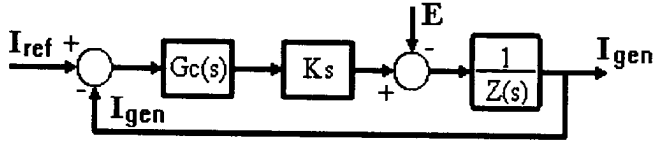


Fig. 8. The block diagram of the current control loop.

where: E is the phase to neutral source voltage,
 $Z(s)$ is the impedance of the synchronous reactor, X_1 ,
 K_s is the gain of the converter,
 $G_c(s)$ is the gain of the PI controller.

The values of K_s and $G_c(s)$ are given in (7) and (8).

$$K_s = \frac{V_{dc}}{2\xi} \quad (7)$$

$$G_c(s) = K_p + \frac{K_i}{s} \quad (8)$$

From Fig. (8) and using (8) the following expression is obtained:

$$I_{gen} = \frac{K_s(K_p + \frac{K_i}{s})}{R_r + sL_r} I_{ref} - \frac{1}{R_r + sL_r} \frac{1}{K_s(K_p + \frac{K_i}{s})} E \quad (9)$$

The characteristic equation of the current control loop is given by:

$$1 + \frac{K_p s + \frac{K_i}{s}}{s(R_r + sL_r)} = 0 \quad (10)$$

The analysis of the characteristics equation proves that the current control loop is stable for all values of K_p and K_i . Also, this analysis shows that K_p determines the speed response and K_i defines the damping factor of the control loop. If K_p is too big, the error signal can exceed the amplitude of the triangular waveform, affecting the inverter switching frequency, and if K_i is too small, the gain of the PI controller decreases, which means that the generated current will not be able to follow the reference current closely.

Simulated results have shown that the compensator transient response is improved by adjusting the gain of the proportional part (K_p) equals to one and the gain of the integrator (K_i) equals to the frequency of the triangular waveform.

B) Dc Voltage Control Loop

In order to eliminate the steady state error in the dc voltage a PI controller is used. The proportional gain and the integral gain are equal to one and 45 Hz respectively (10 times slower than the current control loop).

V.- DESIGN EXAMPLE

To illustrate and facilitate the use of the theoretical results obtained in the previous sections, the following example is given.

The non-linear load (a six-step rectifier) has the following specifications:

S	rectifier rated power	20 kVA
Van	phase to neutral source voltage	220 V

The power circuit components rated values of the three PWM inverters are shown in Table I.

TABLE # 1
RATED VALUES OF POWER CIRCUIT COMPONENTS

	VSI # 1	VSI # 2	VSI # 3
Switching Frequency	450 Hz	970 Hz	1600 Hz
Rated Current	1.1 p.u.	0.11 p.u.	0.07 p.u.
X1	1.738 p.u.	0.813 p.u.	0.494 p.u.

Assuming that the maximum voltage fluctuation in the dc bus is 10 %, the value of the dc capacitor is equal to 2 p.u..

VI.- SIMULATED RESULTS

Figures 9 and 10 show the simulated current and voltage waveforms for steady-state and transient operating conditions. In both cases the active power filter is compensating a six step controlled rectifier. Both figures proves that the active power filter is able to compensate displacement and distortion power factor effectively.

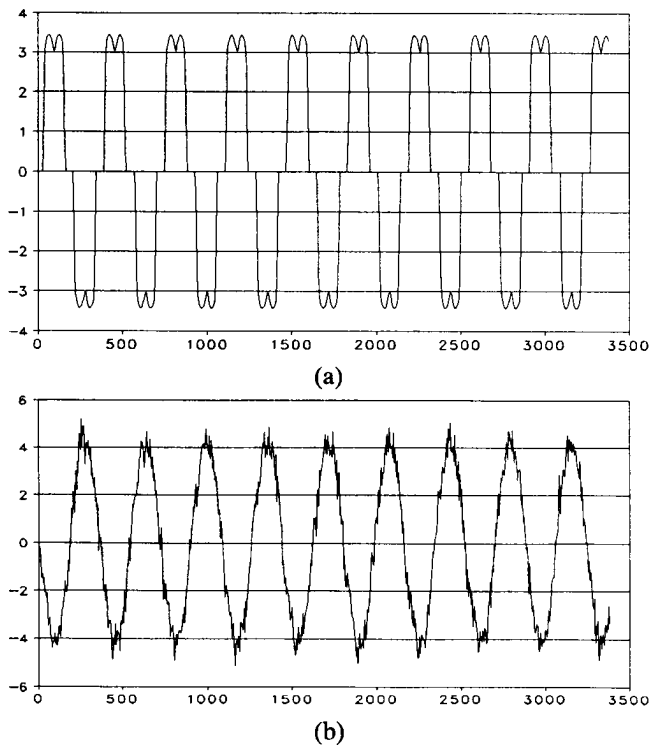


Fig. 9. Simulated current waveforms for steady-state operating conditions. a) The non linear load current. b) The compensated source current.

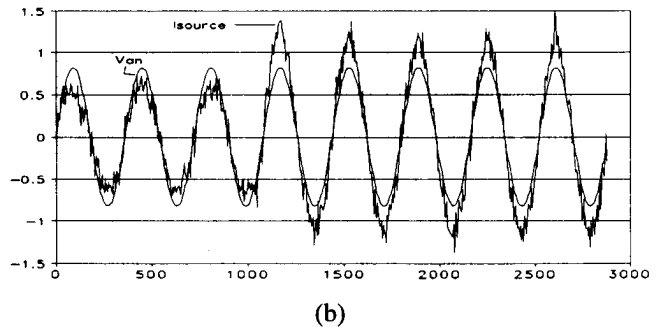
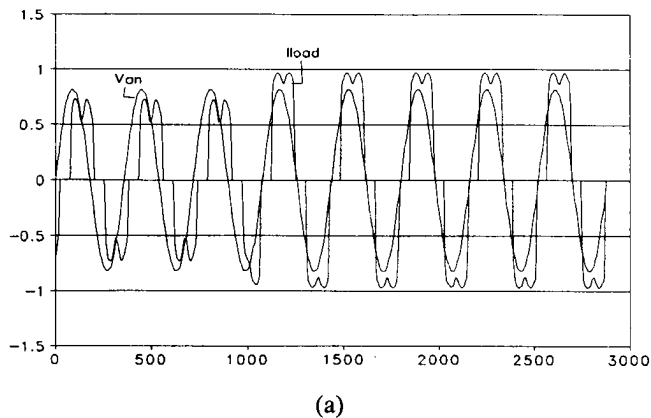


Fig. 10. Simulated current waveforms for transient operating conditions. a) The non linear load current with the respective phase to neutral voltage. b) The source line current and the respective phase to neutral voltage.

VII.- EXPERIMENTAL RESULTS

A 20 kVA laboratory prototype using IGBT switches was implemented and successfully tested in compensating a six pulses controlled rectifier. Steady-state and transient results obtained with this bread board unit are shown in Figs. 11 and 12.

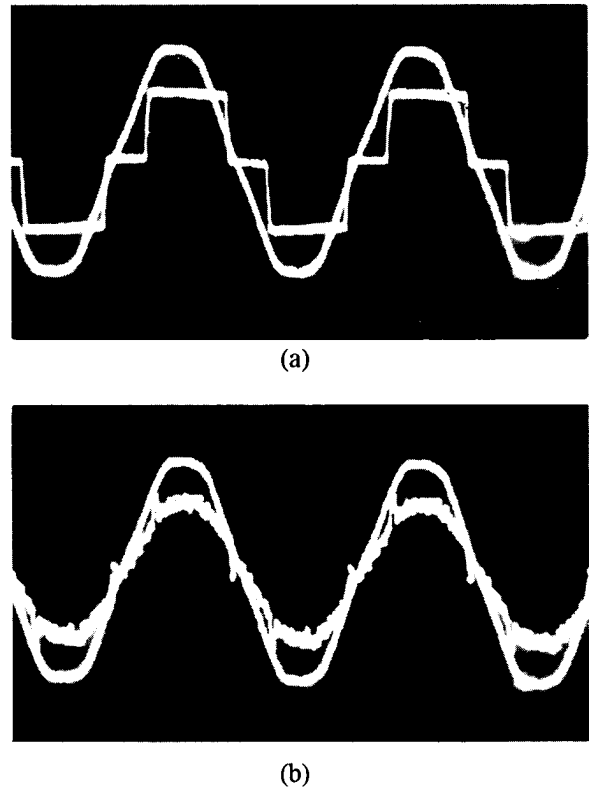
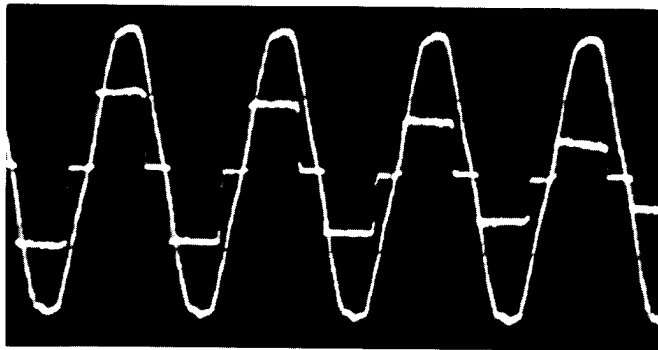
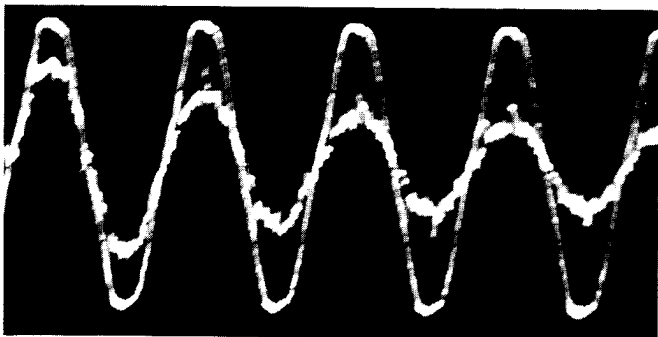


Fig. 11. Steady-state experimental results. a) The phase to neutral source voltage, V_{an} 50 V/div, and the respective load current, 5 A/div. b) The phase to neutral source voltage, V_{an} 50 V/div, and the respective source current, 5 A/div.



(a)



(b)

Fig. 12. Transient experimental results. (a) Phase to neutral source voltage and the load current. (b) Phase to neutral source voltage and the source current.

CONCLUSION

In this paper an active power filter that was implemented with three PWM voltage-source inverters has been presented and analyzed. The proposed system can compensate for displacement and distortion load power factor. Each PWM voltage source inverter operates at a different switching frequency, allowing the compensation of high power non-linear loads. The closed agreement between the analytical and the experimental results proves the validity of the analysis and the feasibility of the proposed system.

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